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IGBT MODULE RELIABILITY

PHYSICS-OF-FAILURE BASED CHARACTERIZATION AND MODELLING

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PAPER A

Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in IGBT modules

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Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in IGBT modules

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ABSTRACT

A micro-sectioning approach for characterizing the quality or degradation state of interconnect interfaces in electronic components is described. The method is presented as a means of investigating the bonding quality of the *Al* wedge bonding process in IGBT modules. But in general it is applicable to any type of interface and may be used to assess the present quality of the interface. The micro-sectioning is based on mechanical polishing, chemical polishing, electro-etching, and various types of microscopy.

1. Introduction

The lifetime and performance of an electronic device as an IGBT (Insulated Gate Bipolar Transistor) module is depending on its application area, often limited by the interconnects. Particularly the interface between the commonly used *Al* bond wires and the semiconductor components is a critical point due to the mismatch in the coefficients of thermal expansion. This mismatch is believed to be the dominating effect in the bond wire fatigue failure mechanism, which includes bond wire lift-off and heel cracking. In recent years the latter has become more and more rare [1–3].

The bond wire lift-off failure mechanism in IGBT modules is primarily due to fatigue crack propagation inside the wire material. This is due to the bonding quality, where the refinement of the granular structure results in a stronger interface than the material itself. Accordingly the crack is initiated in a natural area, near a void or near the interface edge, and propagates towards the wire center where the breaking strength is lower. At some point the grain size of the refinement region comes close to that of the bulk wire resulting in a change of propagation direction of the crack to a horizontal one with respect to the interface. Based on this a microscopical investigation of the wire/chip interface may yield a direct measure of the quality as well as enable a detailed reliability assessment [4,5].

Reducing the risk of interconnect related failure mechanisms is of paramount importance as these are presently the limiting factors. This has motivated a search for an alternative to the *Al* wire as well as to soft solders. To mention a few, the ordinary *Al* wire has been proposed to be substituted by ribbons, *Cu*, or other bonding techniques. These hold various pros and cons, where many of the disadvantages are related to production compared to the wedge bonding applied to *Al* wires. Even though these methods reduce the thermo-mechanical related degradation the interconnects remain to be the weak point with respect to lifetime. Thus, an accurate knowledge of the interfaces is still of importance [6].

This article presents an micro-sectioning approach for characterizing the microscopical processes occurring at interfaces. By investigating the microscopical structure the information regarding quality as well as lifetime may be obtained. In this article, the quality of wire interfaces are investigated for a series of samples to illustrate the method. The grain distribution is derived from the results and used to evaluate the quality of the bonding by looking at the refinement area. Finally, the pros and cons of the method in general are discussed and alternative ideas are presented.

2. Theory

As briefly discussed in the introduction there is a connection between the interface strength and the microscopical structure of the *Al*, more precisely the grain structure of the interface. A concept which is only understood from a fracture mechanical point of view, this is presented briefly in Section 2.1.

Obtaining the grain structure of pure *Al* in a layered system is problematic, as the contrast in the *Al* is often caused by impurities. The contrast across the *Al* is further lowered by all the subjacent layers in the geometry. Therefore, methods like electron backscattered diffraction (EBSD) and electro-etching may be employed to promote the change in crystal structure. This is outlined in Section 2.2.

2.1. Fracture mechanics

The observations that the fractures in the wire/chip interface propagate into the wire away from the interface to a certain point are simply related to the concept of grain size refinement. This is a

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technique used to strengthen certain metals with regard to yield strength and fracture toughness. In general, these properties depend on the grain diameter d, where the relation follows the Hall–Petch equation [7]:

$$\sigma_y = \sigma_0 + k_y d^{-1/2} \quad (1)$$

where σ_y is the yield strength, k_y is the dislocation locking term which describes the yielding properties of a grain to the adjacent ones, and σ_0 is the stress required for dislocation along slip planes. Naturally, the Hall–Petch equation breaks down below certain diameters, but it has been shown to be valid on the nanometer scale [7]. From Eq. (1) it becomes clear that if the fracture toughness follows the same relation, the strength of the bond strongly depend on the refinement region.

2.2. Grain structure in aluminium

The idea of the approaches presented here is to provide images illustrating the grain structure inside the *Al* wire and metallization. For a large number of *Al* alloys this is easily done, as the impurity atoms situate themselves near the grain boundaries. However, in pure *Al* the only difference between grains is a change in crystal orientation. The contrast this provides is not sufficient for optical microscopy or ordinary scanning electron microscopy (SEM).

If one introduces SEM methods like EBSD the grain size and type can be obtained without influencing the structure apart from a standard polishing. The resolution of the SEM also renders it possible to obtain the structure inside the metallization, which is not the case for the method presented later using optical microscopy. However, the disadvantages is the requirement of a SEM with EBSD as well as the amount of time required to obtain the diffraction patterns.

Instead or in combination with EBSD, one may use electro-etching to provide the contrast between the grains in optical images. Here, one uses a reagent to etch the surface and the changes in crystalline structure provide different etching rates. A common approach in pure *Al* is to use an electrolytic procedure with Barker's anodizing reagent on the *Al* surface followed by an investigation using optical microscopy with polarized light. This has previously yielded clear grain structures with a strong color contrast between the different grains, see [8, p. 497]. The reason for the color contrast, however, is a bit unclear. The electrolytic method combined with Barker's reagent is referred to as an anodization, but previous investigations have shown that the increased oxide layers do not provide the optical effects for a contrast between grains. Instead the belief is that the contrast is generated by multiple reflections from a rough surface [8,9].

3. Experimental procedure

The experimental procedure presented in the following is in principal applicable on any given component. The changes necessary are minded towards the region of interest, for instance the electro-etching formulae needs to be changed depending on the material composition of the wire.

3.1. IGBT module

The component of interest is an ordinary high power IGBT module intended as a power converter in e.g. a wind turbine or in the automotive industry. In Fig. 1 the layout of the component analyzed is presented:

A single section of a module consists of a baseplate (3000 μm), a baseplate solder (100 μm), a DCB (1300 μm), 2× diode (300 μm), 2× IGBT (300 μm), and $2 \times 8 - 10$ *Al* wire interconnects (400 μm). Here, the thickness of the given layer is presented in the following brackets. A typical wire layout on the diode in the IGBT module is presented in Fig. 2.

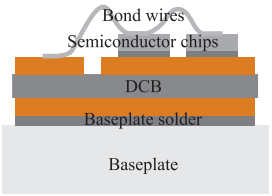

Fig. 1. Cross-sectional geometry of an ordinary IGBT module consisting of a baseplate, a direct copper bonded substrate (DCB), semiconductor chips, and *Al* wire interconnects [2,10].

The layout is similar on the IGBT chip with a larger spacing between the wires, in the type of module regarded.

3.2. Micro-sectioning

The micro-sectioning process may be divided into a macroscopic and a microscopic part. From a macroscopic stand point, the system or module of interest is cut mechanically into single components to reduce the dimensions before the microscopic handling. For an IGBT module this involves isolating the semiconductor components from each other, but also to remove unnecessary layers like a baseplate. The microscopic sectioning includes the fine mechanical polishing to the desired interface, the chemical polishing, and the electro-etching for producing grain structures in the *Al*.

The given chip is cast two times in order to protect the fragile components. If the geometry is to be electro-etched an electrical connection should be made to the metal prior to casting. The procedures are the following:

1. Dividing module into subelements (IGBT, diode, etc.) by mechanical cutting. This may be carried out prior to or after the initial casting into epoxy.
2. Removal of baseplate, baseplate solder, DCB, and semiconductor solder by cutting, diamond polishing, and fine-grade *SiC* polishing. The solders are removed to prevent the layer from affecting the electro-etching and the remaining to simplify the polishing.
3. Second cast and polishing to desired wire interface using fine-grade *SiC* and 3 μm diamond polishing.
4. Chemical polishing for removal of mechanical polishing lines.

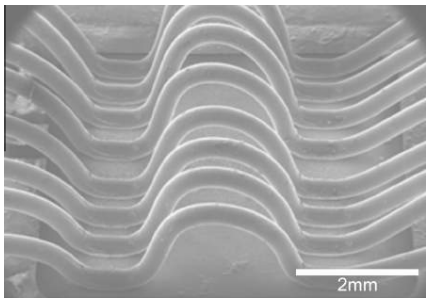

Fig. 2. SEM image of wire layout on top of the diode.

Fig. 3. IGBT chip cast into epoxy and subjected to polishing until a side view of the wire interface is reached.

5. Electro etching of wire/chip interface. Barker's reagent designed for promoting grain structures in pure *Al*. The sample is electro etched with 30 V for 2.5 min with magnetic stirring of the reagent.

An IGBT chip cast into epoxy is illustrated in Figs. 3 and 4.

One should keep in mind that the softness of the *Al* complicates the procedure. During the *SiC* polishing material from the surrounding layers as well as grains from the *SiC* paper may be embedded in the wire. This should be removed in the final 3 μm diamond polishing.

4. Results

The method presented in Section 3.2 is carried out for a series of samples. In general the samples are of the type presented in Section 3.1 with different types of wire. Additional parameters are varied in order to establish a proper quality investigation of the bonding process. These parameters are not subjects of the current investigation. In this paper results obtained using the micro-sectioning approach are presented together with SEM images to illustrate the method and its advantages. Afterwards, a damaged interface is presented to illustrate the reliability possibilities of the approach.

In Figs. 5 and 6 SEM images of *Al* wire bond interfaces are presented. In Fig. 5 the observed wire is on top of the diode whereas in Fig. 6 the interface is on the IGBT. Prior to obtaining the images the wire has been partly pried off to be able to reach the interface.

In Fig. 5 two focused ion beam (FIB) cuts are made into the surface to see the composition inside. The wire print observed is left-over material from the removal of the wire. It was possible to observe the granular structure of both the metallization and the wire in the cross-sectional image of the well produced by the cut.

A similar cross-section is shown in Fig. 6 for the cut made on the IGBT. One can see the leftovers of the wire, the metallization layer, and a part of the silicon chip. Furthermore, the grain structure is visible inside the metallization and wire but with a limited contrast. The void or partly cracked area on the right side is believed to have been created by the prying of the wire.

In Figs. 7 and 8 optical microscopy images of cross-sections of wire bond interfaces obtained through the micro-sectioning approach are presented. In both cases the bond is on top of the IGBT chip which is clear from the trench gate structure seen below the interface.

The image in Fig. 7 is an ordinary bright field (BF) microscopy image, and apart from the gate structure no mentionable objects are apparent.

In Fig. 8 the same type of image as in Fig. 7 is obtained but with electro-etching of the surface and use of polarized light. A clear granular structure is seen where the diameter of the grains ranges in size up to 20 – 40μm. The smallest grains resolved by the microscope are about 5 μm. Furthermore, a clear change in grain structure is observed near the bond interface, which has been partly illustrated with the black line. This is naturally a result of the grain refinement during the bonding process.

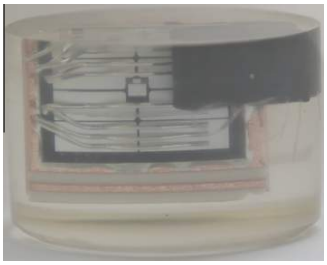

Fig. 4. Top view of the cast presented in Fig. 3.

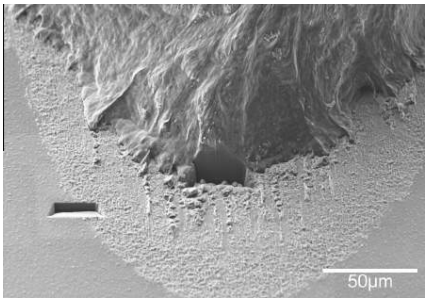

Fig. 5. SEM image of the heel of an *Al* wire bonding. Two FIB cuts has been carried out, one inside the wire interface and one near the edge of the interface after the wire has been pried off.

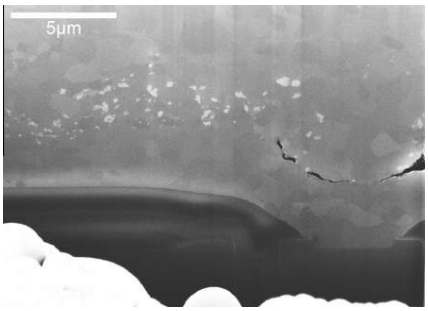

Fig. 6. Image of a FIB cut inside the *Al* wire interface. A clear granular structure is observed inside the metallization as well as the wire. The void observed just above a transistor channel is believed to be created by the prying of the *Al* wire.

In Figs. 9 and 10 cross-sectional images of an interface of a failed module is presented.

In Fig. 9 the interface was observed to be in the initial state of a wire bond lift-off. This is indicated by the delamination of the wire from the metallization, and also the initiation of cracks into the

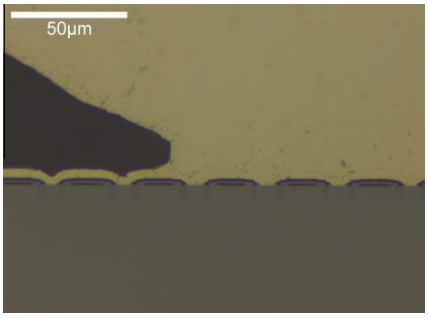

Fig. 7. Ordinary BF microscopy image of the interface between *Al* wire type B and the IGBT chip after micro-sectioning but prior to etching.

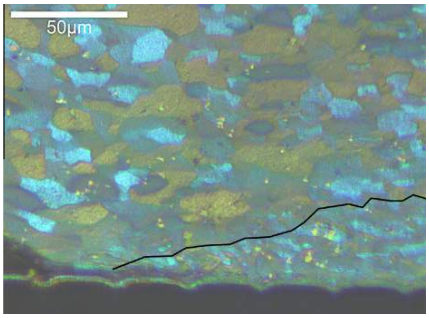

Fig. 8. Microscopy image, of the interface between IGBT and *Al* wire after etching, obtained using polarized light. The solid line is drawn to visualize the interface formed during the bonding.

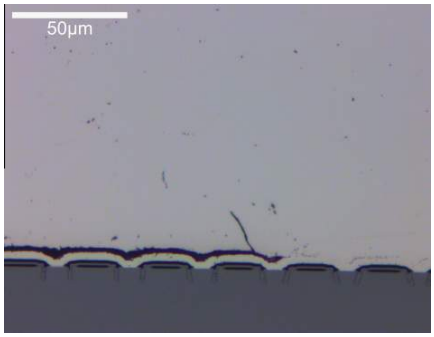

Fig. 9. Cross-sectional image of the heel of a wire bond in a failed module.

wire. The delamination becomes apparent by comparing Figs. 7 and 10.

In Fig. 10 the same interface is presented after being exposed to electro-etching. This has promoted the granular structure of the

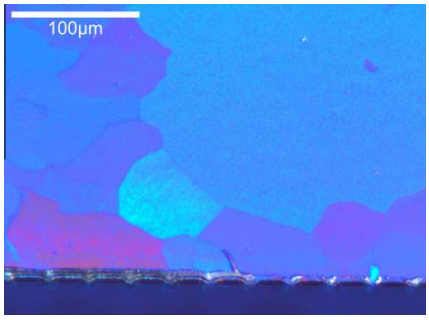

Fig. 10. Cross-sectional image of the sample from Fig. 9 subjected to electro-etching to see the granular structure.

interface, and as discussed in Section 2.1 the fracture is clearly seen to propagate at the grain boundaries.

5. Discussion

The results obtained using ordinary SEM combined with FIB yielded a description of the component composition as well as a high resolution characterization of the grain structure. The size of the wire, however, limits the possibilities. Either the wire needs to be removed before or the characterization is limited to the interface edge. The wire removal was observed to damage the interface, and thereby rendering results unusable. The study of the interface edge is simply not sufficient for a detailed description of the interface quality or state.

Instead, the micro-sectioning approach combined with optical microscopy is proposed for characterization of geometries on this scale. The electro-etched images combined with polarized light provide high contrast showing the granular structure of the interface. This enables the possibility of identifying the grain refinement region and thereby the interface quality. Furthermore, the method was shown to be able to identify failure mechanisms and the present state of the given failure. The identification of the bond quality should be directly usable parallel to module fabrication, and the latter could be employed to establish reliable lifetime estimations. However, the lack of resolution limits the grain structure analysis to the wire itself and an identification of the grain refinement area. Meaning that the investigation of the metallization and similar elements on the same scale must be carried out with more advanced techniques like EBSD.

A final remark on the micro-sectioning approach presented in this paper is off course that all steps are severely damaging to the component in question. And, therefore, the method is not suitable for making many sample investigations during production. But the method shows good applicability to examine selected samples for quality investigation as well as damaged modules for failure identification.

6. Conclusion

A micro-sectioning approach for optical or electron microscopy characterization of interfaces in electronic components is developed and described. This technique includes mechanical cutting, removal of unnecessary parts, mechanical and chemical polishing, and finally electro-etching.

The developed approach gives a possibility to obtain resolution on the μm scale and, in particular, to investigate metal grain structure and possible imperfections in the *Al* wires, and the interface. The method is shown to be able to identify interface related failure mechanisms as well as the present quality of the interface. However, to go to higher resolution (below 1 μm), e.g. inside the chip metallization more advanced techniques like EBSD are needed.

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References

[1] Kanert W. Microelectron Reliab 2012;52:2336–41.
[2] Schilling O, Schfer M, Mainka K, Thoben M, Sauerland F. Microelectron Reliab 2012;52:2347–52.
[3] Czerny B, Lederer M, Nagl B, Trnka A, Khatibi G, Thoben M. Microelectron Reliab 2012;52:2353–7.
[4] Goehre J, Schneider-Ramelov M, Geissler U, Lang K. In: CIPS, 3.4.
[5] Geiler U, Schneider-Ramelow M, Reichl H. IEEE Trans Compon Packag Technol 2009;32:794–9.
[6] Guth K, Siepe D, Görlich J, Torwesten H, Roth R, Hille F, Umbach F. In: PCIM Europe. p. 232–7.
[7] Hansen N. Scr Mater 2004;51:801–6.
[8] Voort GV. ASM handbook. ASM international of etallography and microstructures, vol. 9; 2004.
[9] Perryman E, Lack J. Nature 1951;167:479.
[10] Lutz J, Scheuermann U, Schlangenotto H, Doncker R. Semiconductor power devices – physcis, characteristics, reliability. Springer-Verlag; 2011.

PAPER B

Interface structure and strength of ultrasonically wedge bonded heavy aluminium wires in Si-based power modules

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Interface structure and strength of ultrasonically wedge bonded heavy aluminium wires in Si-based power modules

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Abstract In this paper the microscopical structure of wedge bonded interfaces is investigated, with a focus on what effect the power in the ultrasonic bonding and the initial microscopical structure of the *Al* wire have on the quality of the bonding. The quality evaluation is based on mapping the microscopical restructuring of the wire grains during bonding and thereby assessing the effective bonding area. Three approaches are utilized in the interface characterization: mechanical shear test, optical microscopy combined with micro-sectioning, and scanning electron microscopy assisted by focused ion beam milling. The shear test is applied to quantify the strength of the bonded interfaces, while the other methods are used to map the grain reconstruction caused by the bonding. From the results it is possible to map a 3D image of the wire deformation, and the grain refinement region which is the dominating parameter with respect to fatigue related cracking of the interfaces. It is found that the bonding power, as well as the initial wire structure directly affects the refinement region and thereby the strength of the interface.

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1 Introduction

For several decades bonded wires have constituted a significant percentage of the interconnections in *Si* based power modules. In the last years the common approach for wire bonding has been ultrasonically wedge (US) bonding. And for quite some time, heavy *Al* wire bonds have been the dominating interconnection technology in high power converters [1, 6, 7, 13, 15].

The high quality of the present semiconductor components makes interconnects one of the weak elements in power modules. Furthermore, the ever increase in semiconductor component performance and capability place additional load on the interconnections. Also the introduction of new types of semiconductor materials like *GaN* or *SiC* which may operate at higher temperatures than conventional *Si*-based insulated gate bipolar transistors (IGBT) sets new requirements for bonding technology [1, 2, 5].

Generally, the US bonding process is believed to be a solid state process, which is supported by several arguments. The bonding is normally carried out at room temperate and investigations have shown limited temperature changes during the bonding [11, 13].

The bonding is carried out in a series of overlapping phases: (1) hardening of the wire by applying a force through the wedge. (2) Reducing the yield and tensile strength of the *Al* wire by ultrasonic vibrations. A process normally called ultrasonic softening. (3) Deformation of the wire created by the two previous processes which enables diffusion and removal of impurities. The diffusion mentioned here is typically observed if the wire is not pure *Al*. (4) Ultrasonic hardening of the wire following the softening. The combination of the phases result in an adhesion process ending up in a polycrystalline interface [6, 9, 11–13].

The US bonding of an *Al* wire on top of an *Al* metallization yields a so-called refinement area around the interface, where the original grain structure of the wire and metallization is refined into grains depending on the applied power and the original structure.

1.1 Wire bond strength

The characteristics constituting a quality wire bonding can be specified in several ways. Some of the relevant approaches are briefly discussed below.

In [6] 25 µm *AlSi1* wire was US bonded to different types of pads with varying US power. The interfaces were studied using focused ion beam (FIB) to produce cross-sections of the wire/pad connection. It was observed that an increase in US power resulted in decrease of grain sizes in the wires near the interface and increase of the area of the reformation zone around the interface. In other words, a higher US power reformed additional grains further away from the interface. This is consistent with the results from [13] were the footprint structure of US bonded 25 µm *Al* wire was investigated. Wires were bonded to selected pads with varying US power followed by a mechanical lift-off of the wires. The residual material on the pads was used to estimate the shape of the bonded interface and the extent of a proper bonded wire. The residual material was found in an elliptical shaped footprint, where the volume of material was proportional to the bonding power. In [1] two types of 375 µm *Al* wires, 99.999 and 99.99 % purity, were bonded to *Al* metallization on an *Si* die. The quality was investigated through a number of thermal cycles of a sample followed by a shear test and scanning electron microscopy (SEM) combined with FIB cross-sectioning. The wire with the highest purity showed a significantly higher durability. The reason for this interface to be more robust was ascribed to the fact that it only had a single area of natural crack propagation. The FIB cross-sections were primarily used to investigate any changes in the grain structure over time due to the thermal load. The result was a clear tendency of grain coarsening due to annealing at high mean temperatures.

1.2 Bond wire fatigue

Failure mechanisms related to the wire interfaces in power modules are usually referred to as bond wire fatigue [2, 3, 10]. Bond wire fatigue is primarily separated into bond wire lift-off and heal cracking. Which one is relevant depends highly on the power load and the large scale geometry of the module. In both cases the failure mechanism is induced by temperature changes. The temperature fluctuations are created by the oscillatory nature of the load experienced by power converters [7, 10, 15].

Bond wire lift-off or cracking have been studied extensively in different ways. The conventional way has been to subject a given component to either thermal-, power-, or mechanical cycling until failure and investigate the outcome. This has led to knowledge regarding the importance of the curvature of the wire and the geometrical position of the interfaces [1, 4, 16]. However, the importance of these parameters is primarily linked to the stress experienced by the interface, and not the microscopical fracturing process. Depending on the application of the component a number of processes may be significant like diffusion, recrystallization, material expansion, and so on. In all cases, however, the thermal cycling experienced by electronic components creates a stress in the layered structure. The strength of an US bonded wire is therefore directly limited by its microscopical structure.

The importance of the microscopical structure becomes clear when regarding the lift-off process. Due to the geometry or large temperature cycles, the stress in certain regions may exceed the elastic limit thereby creating plastic deformations. Over time, cracks are initiated at natural sites like voids or at the interface heel. Due to the strength of the crystalline grains cracks are expected to propagate at grain boundaries [7, 14]. The result is that cracks are often observed initiated near the interface and propagate inwards the wire where the grain diameter increases. The reason for this can be explained from the Hall–Petch relation:

$$\sigma_y = \sigma_0 + k_y d^{-1/2} \tag{1}$$

where σ_y is the yield strength, k_y is the dislocation locking term, d is the grain diameter, and σ_0 is the yield strength for dislocation along slip planes [8, 14]. Due to the decreasing of fracture toughness when the diameter increases a crack moves from the interface and inwards the wire. However, the effective stress normally decreases when moving away from the wire/chip interface. This means that a given distance from the interface, an equilibrium between fracture toughness and effective stress is reached limiting further propagation in the vertical direction. Then the crack should propagate in the direction parallel to the chip surface or interface until the wire lifts-off [7].

In the current paper the quality and strength of interfaces are investigated for heavy *Al* wires US bonded to an *Al* metallization, which is a standard layout in high power converters. The interface is investigated for wires of two different microscopical structures for bondings created with three different power settings within realistic production range. The strength and quality evaluation of the bonds and interfaces are carried out using a standard shear test, optical microscopy based on an micro-sectioning approach, and SEM.

Fig. 1 Image of one of the test samples. Ten *Al* wires are bonded to an IGBT chip, a diode chip, and the *Cu* of the DCB

2 Samples

The investigation is focused on two types of 99.99 % pure 400 μm *Al* wires US bonded to a standard direct copper bonded (DCB) substrate with semiconductor components, see Fig. 1.

Two types of semiconductor components are present, as in typical power converters, namely standard IGBT and diode chips, where the former are the larger chips in Fig. 1. Ten parallel *Al* wires are bonded to the chips and the DCB. The two types of wires are manufactured by different companies and are denoted as wire A and B from this point and onward. For a description of the US bonding process or the standard layout see [17, Ch.2].

The main interest with regard to strength of the bonded interface is the initial composition of the wire and the power applied during the US bonding [13, 17].

Wire A and B were US bonded with the same force but three different power settings. In total this yields six samples of two wire types bonded with varying power. The samples are denoted: A_1-A_3 and B_1-B_3. Subscripts indicate the increase of the bonding power in three steps from a relative value 1.0–1.5. Total process time per wedge are 105 ms where the force and power is ramped to the final value. The bonder used is a 3600 plus from Kulicke & Soffa with rear cut configuration and a standard bonding tool. During bonding the wire deformation is measured. For sample A the mean wire deformation height ranges from 97 to 124 μm and for B from 92 to 118 μm.

3 Experimental procedure

Three different methods are used to investigate the strength of the US bonded interfaces: a mechanical shear test, the so-called micro-sectioning approach, and SEM combined with FIB milling.

3.1 Shear test

The most common method to quantify the quality of a large wire bond on top of an active surface, like an IGBT, is the wedge shear test. For the tests a Condor Classic bond tester of Xyztec was used.

To perform the shear test a tool is positioned behind the wedge. After an automatic touch down the tool moves upwards to the predefined shear height (10 % of wire diameter) and then shears the wedge. The maximum force measured while shearing the wedge is the shear value. In addition to the shear value the *Al* residue of the wedge was valued. Therefore the percentage of *Al* remaining in the shear height layer is visually determined. Both the residue and the shear value describe the quality of a large wire bond. There exist other possible values which can be taken into account like the pull value, the wedge width, or data collected during the bond process.

3.2 Micro-sectioning

To investigate the microscopic structure of the wire/chip interfaces a micro-sectioning approach was utilized. The process is described in detail in [14], where similar interfaces were investigated. To summarise, reaching the interface of interest is done in a series of steps:

1. Embedding sample in epoxy for protection.
2. Mechanical cutting for removal of the material (Cu and ceramic) surrounding the chip/wire interface of interest.
3. Rough polishing for removal of layers underneath chips, followed by a second embedding in epoxy.
4. Fine grade polishing from the side or the end of a wire interface until reaching the wire.
5. Polishing with 1–3 μm particles for removal of large polishing stripes.
6. Chemical polishing.
7. Electro-chemical etching in Barker's reagent (electro-etching) of the interface to promote grain structure contrast, in the microscope, of the *Al* wire material.

All samples are handled identically in the micro-sectioning process, except for the electro-etching. As the wires are different in the grain structure from the beginning, type A require a longer etching time, app. 3 min, to provide enough contrast between grains, whereas type B only needs app. 2 min. To visualise the granular structure the samples are placed in an optical microscope under polarized light. The microscope is an inverted Leica DMI3000M with and added polariser and analyser before and after the sample, respectively. In our case the polariser and analyser are placed perpendicularly for maximum contrast [14, 18].

3.3 SEM and FIB

The micro-sectioning approach is limited by the resolution of the optical microscope and the contrast between grains.

Table 1 Shear test results

	A_1	A_2	A_3	B_1	B_2	B_3
Residue (%)						
0				2		
≤20	1			5		
≤40	4			8	2	
≤60	3	2		4	2	1
≤80	3	5	2	1	7	4
≤100	9	13	18		9	15
Value						
$\bar{x}[N]$	25.75	26.48	26.49	25.28	27.79	28.15
$\sigma[N]$	1.45	0.70	0.65	1.85	0.69	0.80

$\bar{x}$ and σ are the mean and standard deviation of the shear values

This resolution is found to be insufficient to map the grains in the metallization layer. The grains become smaller in the wires close to interface, thus requiring a method with better resolution. Therefore, SEM combined with FIB is used to characterize the refinement area closest to the chip surfaces, as well as the metallization layer. Since the available FIB equipment has a limited milling range, the wire is partly pulled of prior to the milling. The SEM/FIB utilized is a Zeiss 1540 XB. For additional information as well as images regarding the sample preparation for FIB milling see [14].

4 Results

All six types of samples were investigated using shear test and micro-sectioning. Apart from this a selected number of samples were characterized using SEM.

4.1 Shear test

In Table 1 the results from the shear test are presented. The test itself is carried out on 20 bonded wires on each of the six samples presented in Sect. 2. After removing the wire, the residue material in the bond footprint is compared to an ideal bond and split into groups of 20 %.

It is clearly seen from Table 1 that for both types of wires the strongest interface is gained by bonding with the highest power. Wire type A yields higher percentage of residue compared to wire type B that indicates higher degree of refinement. In contrast, however, sample B require a higher shear force.

4.2 Micro-sectioning

From Fig. 1 it is clear that each wire has five interfaces: two on the IGBT, two on the diode, and one on the DCB. Apart from the change in layer composition, the types of bondings are commonly divided into end- and stitch bondings. The final interface on top of the IGBT and the *Cu* connection are end bondings, and the remaining are referred as stitch [1]. Apart from dividing the bondings into stitch and end, the change in layers constituting the bond separates the interfaces into three more types: $Al^{(w)}/Al^{(met)}/Si^{(IGBT)}$, $Al^{(w)}/Al^{(met)}/Si^{(Diode)}$, and $Al^{(w)}/Cu$. As earlier discussed we are primarily interested in the strength of the interface regards normal wear-out failures. Therefore, only the $Al/Al/Si$ interfaces are presented in his paper.

Two micro-sectioning approaches are utilized in the paper: side- and end view cross-sectional images. The former is a cross-sectional longitudinal image obtained by polishing parallel to the wire length. The second is a diametrical one. Both cases yield an image of the wire shape, grain structure, and deformation lines but with different views. Both methods are applied to wire samples before bonding. The wire grain structure of these samples is found to be the same as the structure of bonded wires outside the interface region. For the wire/IGBT interfaces the approaches are carried out for all samples. Whereas for the wire/diode interfaces the investigation is limited to side views of all samples and selected end views. Only a limited number of diode samples are regarded as US bonding on top of the smooth diode surface is normally easier than the rough IGBT surface.

In Fig. 2a, b end view images of wires A and B, respectively, are presented. The cross-sections illustrate the wire structures in the initiation of the wire/IGBT interface. In these images the refinement area is clearly observed near the IGBT surface. However, any refinement and strain lines are limited to the immediate proximity of the IGBT surface. The granular structure in the center of the wires is the same as in the wire prior to bonding. Here the structural difference is observed between wire type A and B, the former has large grains ranging from 10 to 70 µm, whereas the grains in type B range from 5 to 20 µm. As would be expected, only a limited deformation of the circular wire structure is observed. The difference in wire grain structure prior to bonding explains the difference in deformation during bonding as the hardness of wires consisting of smaller grains is higher [8].

In Fig. 2c, d the same two samples are presented, but now the position of the cross-section is closer to the center of the wire/IGBT interface. In contrast to the initiation of the interface the granular structure presented in Fig. 2c, d is clearly affected by the bonding process. Refined areas are observed near the interface. These areas have a lens-like shape, i.e. deeper refinement in the wire around the middle and more shallow at the edges. In Fig. 2c the refinement area is much more well-defined than in Fig. 2d. However,

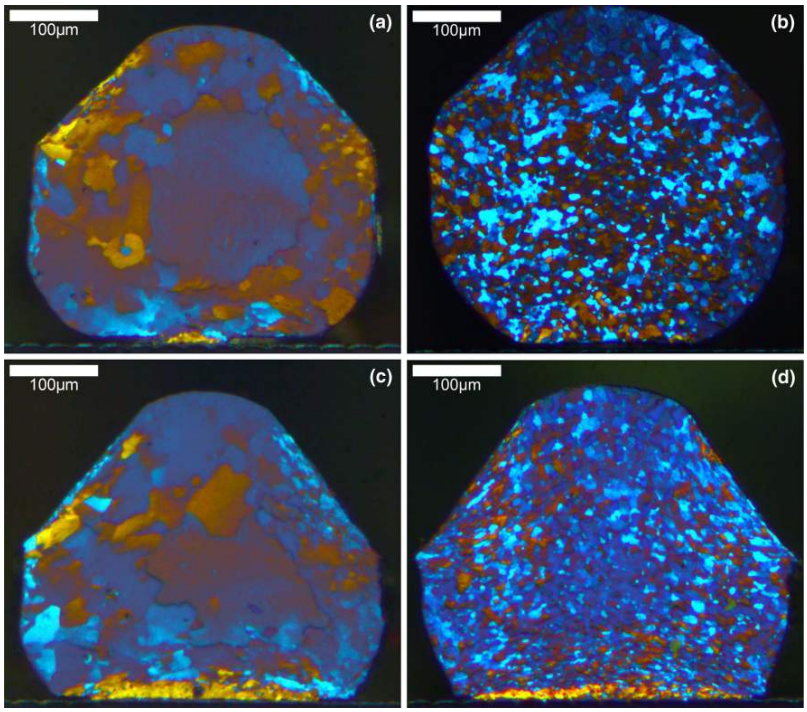
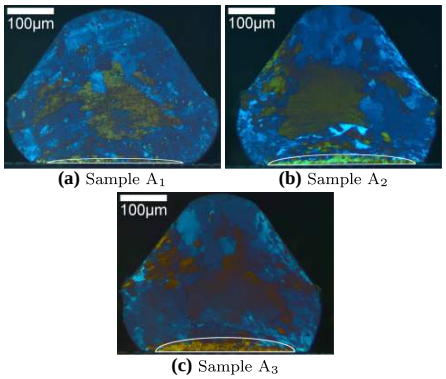


Fig. 2 End view images of samples A_3 and B_3 close to the initiation (**a**, **b**) and around the middle (**c**, **d**) of a wire/IGBT interface

this is primarily due to the large size difference between the bulk grains and the refined grains, that creates an increased contrast in the optical images. Above the refinement areas transition regions are observed. The effect is mostly pronounced for wire B, see Fig. 2d, where grain deformation can be seen close to the center of the wire. The grain deformation lines are generally observed to flow from the center of the wire and outwards which is consistent with the deformation of the wire geometry. The difference in initial grain structure of wire A and B makes it difficult to directly compare the quality of the interfaces from the refinement regions. Estimating a strict height of the refinement region in the center of the interface could be a parameter describing the bond quality. However, the passing from the strongly refined area to the deformed area is a gradual transition making it difficult to estimate such a height.

In Fig. 3 three images of the wire/IGBT interfaces for samples A_1-A_3 are shown. The refinement area is approximated with half an ellipse based on the grain size. It is difficult to directly compare the images of A_1-A_3, as it is evident from the 3D reconstruction in Fig. 4 that the height and width of the refinement area depends on the position of the cut. But based on the wire shape and height, these cuts are estimated to be close to the same position in the interface. From this simple estimation of the refinement area there is a clear tendency that a higher power during the US bonding creates a larger refinement area. The tendency is the same for wire B, but with a smaller difference between samples.

By combining a series of cross-sections of the same wire interface a 3D reconstruction of the wire structure, the bond footprint, and the refinement area are obtained. In Fig. 4 an image of half an interface of the B_1 sample is presented. The refinement area has been approximated with half an ellipse corresponding to the largest grain refinement occurring in the center and decreasing towards the edge. Eight cross-sectional images inside the interface were



(a) Sample A_1 **(b)** Sample A_2

(c) Sample A_3

Fig. 3 End images of the wire near the middle of the wire interfaces. The refinement region is approximated with half an *ellipse*

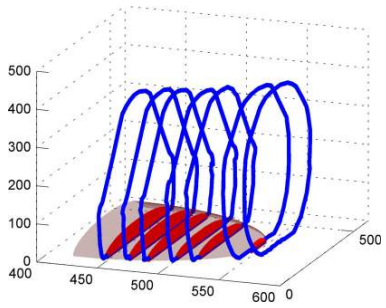


Fig. 4 3D reconstruction of a B_1 wire/IGBT interface, the grain refinement region approximately spans half an *ellipsoid*

combined for the 3D reconstruction, but only six are included to simplify the plot. The most right closed loop corresponds to the image obtained outside the interface. In accordance with [13] the bond footprint is seen to be shaped as an ellipse. The footprint widens towards the center of the interface, and the height of the refinement area increases towards the center. By combining these two tendencies the area of the wire constituting the refinement region of the bonding is seen to span half an ellipsoid.

In Fig. 5 a side view image of the wire on top of the diode in sample B_3 is presented. The wire grain structure can be divided into three primary regions: the refinement-, the deformation-, and the original region. Grains in the refined area are so small that they are not easily distinguished on this scale. The deformation area is somewhat more easily observed. Especially in Fig. 5b, c where a significant part of wire has been deformed towards the diode surface during the US bonding but without obtaining an actual bond.

4.3 Grain structure in chip metallization

In Figs. 6 and 7 cross-sectional SEM images of FIB cuts into the wire/metallization interface on top of a diode of sample B_1 are presented. The images are obtained by partly prying of the wire followed by FIB milling. Figure 6 is obtained by milling the center of the wire/diode interface, whereas Fig. 7 corresponds to the edge of the bond footprint. The vertical lines in both images are artefacts from the FIB milling.

In the very bottom of Fig. 6 one can see *Pt* particles formed at the interface during the diode fabrication. Above that the grainy structure is found and the size of the grains are clearly seen to decrease towards the interface with the wire. By comparing Figs. 6 and 7 it is clear that the grains observed in the metallization layer are created during the bonding. At the edge of the bond footprint, see Fig. 7, the original polycrystalline structure as well as the transition region are presented. There are no grains observed there. Thus, one can conclude that the metallization also experiences reconstruction from original (outside the interface) to granular-like one (at the interface) during the wire bonding.

5 Discussion

The discussion of the results presented in Sect. 4 is separated into two parts: a general discussion of the structure of a wire bonding and the effect of the wire structure combined with the variation of power.

5.1 Wire bonding structure

US bonding of pure heavy *Al* wires to an *Al* metallization yielded, regardless of sample type and fabrication method, very similar characteristic interfaces. In general, the interface can be divided into two regions: the refinement area and deformation region.

The refinement region is the essence of the bonding process. It is the backbone of the solid connection process, determining the robustness of the wire connection in real life operation. From the images presented in Figs. 3 and 5 it was possible to approximate the shape of the refinement region with half an ellipse. By combining this with the elliptically shaped bond footprint it was possible to reconstruct a 3D structure of the refinement region and the wire deformation in general, as shown in Fig. 4. The

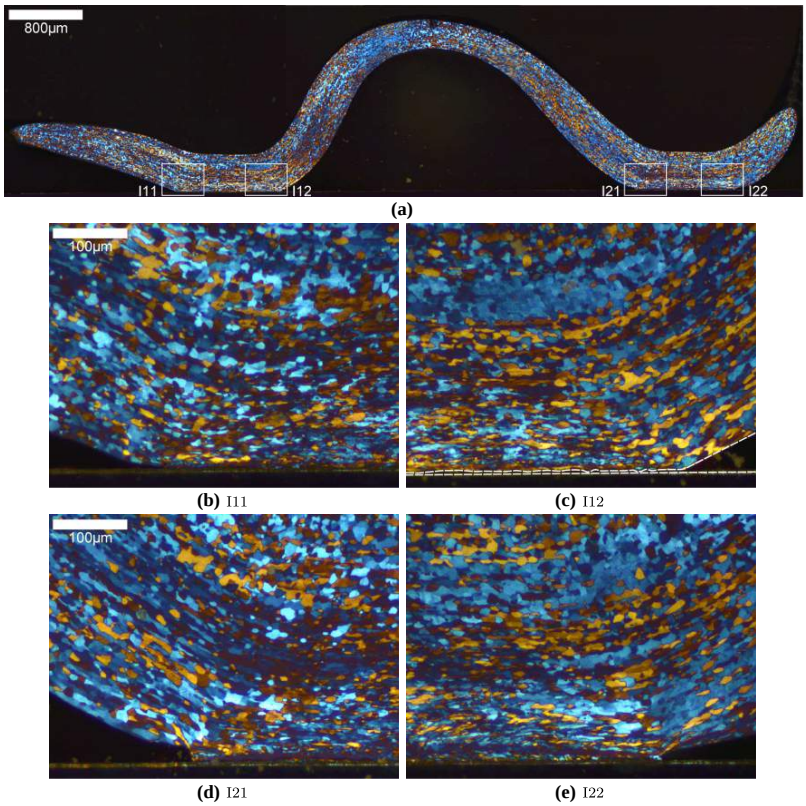


Fig. 5 **a** Side view image of the wire curve on top of the diode from B_3. **b–e** Magnified images of the interface corresponding to the inserts shown in **a**. *Dashed line* in **c** is given for better visualization of the junction between the wire and metallization. See text for details

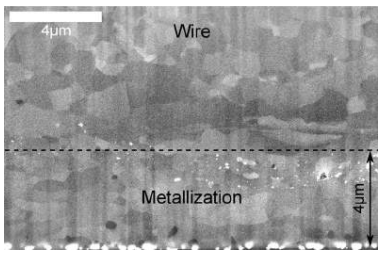


Fig. 6 SEM image of the wire/metallization/diode interface of sample B_1. The *white spheres* at the *bottom* of the image are *Pt* particles on *top* of the diode

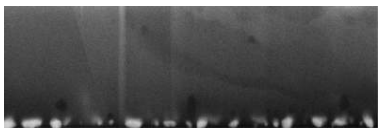


Fig. 7 SEM image of the metallization near the edge of the bond footprint

elliptic shape of the bond footprint and the side views are in accordance with earlier studies, see [6, 13], respectively. The volume of the half ellipsoid corresponding to the refinement region gives a direct estimation of material with

changed structure. Furthermore, by combining the deformation of the wire shape with the ellipsoid volume it is possible to estimate the effectiveness of the bonding parameters.

In a bonded wire there was a tendency that the grain size is significantly decreased at the interface and then gradually increases towards the center. There is a similar tendency found in the metallization layers. Directly underneath the wire bonding a granular structure is observed. This, however, only reach the edge of the bond footprint where the grains vanish and only strain lines from the bonding process are present. Outside the footprint the original polycrystalline *Al* film is still present. These changes inside the metallization might affect the lifetime of the layered structure in real life operation.

The deformation region in a wire is much more vague than the refined area, as it varies from clearly deformed grains to areas only containing plastic flow lines. Highly deformed grains are primarily observed directly above the refinement area, whereas the flow lines reach far into the center of the wire. In wire B the plastic flow lines expand above the center of the wire in the middle of the interface which is in accordance with the interface structure depicted in Fig. 4. These lines follow the process of the bonding, where the plastic slip initially occurs towards the interface and then outwards when the connection with the metallization is initiated. From Fig. 5 it is also evident that the deformed region can propagate in the wire quite far from the actual interface. By comparing interfaces *I*1 and *I*2 in Fig. 5 it is apparent that different geometries exist for the same wire and the same type of bonding. As can be seen in Fig. 5b, c, the wire is highly deformed and almost touching the metallization (the gap is only a couple of μm) approximately 100 μm outside the interface. The lack of bonding is marked with a dashed line in the latter image. In the second interface the bonding ends abruptly as seen in Fig. 5d, e. This would not affect the shear test results, but these two interfaces may perform differently under real operating conditions.

The reason for the difference between the refinement and deformation regions is related to the ultrasonic bonding process which leads to softening of the grains initiates in the contact area between the wire and chip surface. This softening effect decreases when moving away from the chip surface towards bulk wire, at some point this effect is no longer adequate for grain refinement at the given force. The result is a grain deformation instead of an actual grain refinement. As the grain strength is determined by its diameter, see Eq. (1), the decreasing softening effect also causes the increasing grain diameter. At, the fixed applied force and decreasing softening limits the grain refinement during bonding to a size which is increasing with the distance from the interface. By increasing the ultrasonic power the refinement region develops deeper into the wire bulk.

5.2 Variation of wire structure and applied force

The difference in wire structure creates a significant difference in quality of the final wire bonding. In Fig. 2 end view cross-sectional images are presented for both types of wires. From the Hall–Petch equation (1) it is apparent that smaller grains are harder to refine. Thereby wires of type B require higher force or ultrasonic energy to provide a proper bonding. Applying additional force or energy, however, is limited by other factors. Additional force always poses the risk of damaging subjacent layers, like the metallization, semiconductor chips, or solders. Furthermore, additional ultrasonic energy might not necessarily yield additional softening, as it is well known that the application of ultrasonic energy primarily affects the impurities of the solid [9, 11, 12].

From the shear test results in Table 1 it is clear that an increased power during production apparently yields a better result. This can be explained using Fig. 3, where the refinement area is seen to increase with the power. Therefore, the increased volume of the refinement area would indicate a stronger interface. But, as apparent from Fig. 5, grain deformation regions can extend far beyond the interface making it necessary to limit the bonding parameters. It was difficult to extract a particular relation between the extent of the deformation beyond the interface and the applied power. However, the studies indicate that the deformation region extends outside the interface more in the samples made under lower power conditions. This could be explained by the applied bonding parameters not being sufficient near the edges to create a bond, but enough to deform the grains. Thus, the settings can be increased to provide better bonding quality but this should not reach the point where metallization or semiconductor components are damaged. Further investigations are needed to estimate these limits.

The difference in initial grain structure explains why wire A yields a better result than wire B in the shear test with regards to residual material and why wire B require a higher shear force. Samples A and B are bonded with the same applied parameters, but in Table 1 sample A has a significantly better result with respect to the amount of residual material. This is accredited to the grain refinement process. In both samples the grain size increases gradually from the metallization interface towards the wire center. However, in A the grains are significantly refined near the metallization compared to the original structure, and therefore the transition from the refinement region to the deformed region is nearly abrupt. This is not the case for wire type B, where the transition is nearly continuous until

reaching something resembling the original grain structure. However, it needs to be mentioned that wire A is not necessarily more reliable and robust in field use. As discussed in the introduction, the common failures of wire interfaces in power electronics are thermomechanically created. The fracturing of the interfaces depend on the propagation of cracks inside the interfaces, and here the initial small grain structure of wire B could yield an advantage due to the Hall–Petch relation.

6 Conclusion

Interfaces of heavy *Al* wires ultrasonically wedge bonded to metallization layers in high power electronics modules are studied using shear test, optical microscopy combined with micro-sectioning and SEM assisted by FIB. Two different types of wires bonded at a few selected power settings (typical for the production process) are under investigation. Main difference in the micro-structure of the wires is found to be a grain size which varied between 10 and 70 μm for type A and between 5 and 20 μm for type B.

A 3D map of the bonded wire deformation is developed. One of the dominant parameters of bonding is formation of refinement regions close to the interface in both types of wires. The refinement region is characterized by significant reduction of the grain sizes. Increase of the applied power during bonding leads to considerable expansion of the refinement region inwards the wire in the shape of an half ellipsoid. Behind the refinement region grains start enlarging through the so-called deformation region gradually reaching sizes typical for original wires. Much sharper transitions between the refinement and deformation regions are found for wire type A compared to B. On the other hand, the deformation region extends deeper in the wire bulk for type B than for type A showing also clear plastic flow lines formed during the bonding. Shear tests show considerably better robustness for wire type A, with respect to the refinement region. Comparing the bonding of wires A and B with identical applied power during the bonding one can conclude that the strong refinement, which is well-pronounced for wire type A, is one of the key points for the bond strength and high robustness of the interface.

It is worth noting that the metallization layer also undergoes refinement. The formation of grains is found beneath the bonding interface while outside the edge of the bond footprint the original polycrystalline structure (without grains) of the metallization is observed. One can suggest that this refinement is also important for the robust bond formation. However, more detailed study is required to evaluate this restructuring.

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References

1. P. Agyakwa, M. Corfield, L. Yang, J. Li, V. Marques, C. Johnson, Microstructural evolution of ultrasonically bonded high purity Al wire during extended range thermal cycling. Microelectron. Reliab. **51**, 406–415 (2011)
2. M. Ciappa, P. Malberti, W. Fichtner, P. Cova, L. Cattani, F. Fantini, Lifetime extrapolation for IGBT modules under realistic operation conditions. Microelectron. Reliab. **39**, 1131–1136 (1999)
3. B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, M. Thoben, Thermo-mechanical analysis of bonding wires in IGBT modules under operating conditions. Microelectron. Reliab. **52**, 2353–2357 (2012)
4. B. Czerny, I. Paul, G. Khatibi, M. Thoben, Experimental and analytical study of geometry effects on the fatigue life of Al bond wire interconnects. Microelectron. Reliab. **53**, 1558–1562 (2013)
5. P. Dietrich, Trends in automotive power semiconductor packaging. Microelectron. Reliab. **53**, 1681–1686 (2013)
6. U. Geissler, M. Schneider-Ramelow, H. Reichl, Hardening and softening in AlSi1 bond contacts during ultrasonic wire bonding. IEEE Trans. Compon. Packaging Manuf. Technol. **32**, 794–799 (2009)
7. J. Goehre, M. Schneider-Ramelov, U. Geissler, K. Lang, Interface degradation of Al heavy wire bonds on power semiconductors during active power cycling measured by the shear test, in *Conference on Integrated Power Electronics Systems, 3.4* (2010)
8. N. Hansen, Hall–Petch relation and boundary strengthening. Scr. Mater. **51**, 801–806 (2004)
9. G. Harman, J. Albers, The ultrasonic welding mechanism as applied to aluminium- and gold-wire bonding in microelectronics. IEEE Trans Parts Hybrids Packaging **13**(4), 406–412 (1977)
10. W. Kanert, Active cycling reliability of power devices: expectations and limitations. Microelectron. Reliab. **52**, 2336–2341 (2012)
11. J. Krzanowski, A transmission electron microscopy study of ultrasonic wire bonding. IEEE Trans. Compon. Hybrids Manuf. Technol. **13**, 176–181 (1990)
12. B. Langenecker, Effects of ultrasound on deformation characteristics of metals. IEEE Trans. Sonics Ultrason. **13**(1), 1–8 (1966)
13. I. Lum, M. Mayer, Y. Zhou, Footprint study of ultrasonic wedge-bonding with aluminum wire on copper substrate. J. Electron. Mater. **35**, 433–442 (2006)
14. K. Pedersen, P. Kristensen, V. Popok, K. Pedersen, Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in IGBT modules. Microelectron. Reliab. **53**, 1422–1426 (2013)
15. S. Ramminger, P. Trkes, G. Wachutka, Crack mechanism in wire bonding joints. Microelectron. Reliab. **38**, 1301–1305 (1998)
16. U. Scheuermann, R. Schmidt, Impact of load pulse duration on power cycling lifetime of al wire bonds. Microelectron. Reliab. **53**, 16871691 (2013)
17. A. Volke, M. Hornkamp, in *IGBT Modules—Technologies, Driver and Application* (Infineon Technologies, 2011). ISBN 978-3-00-032076-7
18. G.V. Voort, *ASM Handbook: Volume 9: Metallography And Microstructures* (ASM International, Metals Park, 2004)

PAPER C

Degradation Assessment in IGBT Modules using Four-Point Probing Approach

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Degradation Assessment in IGBT Modules using Four-Point Probing Approach

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***Abstract*—Four-point probing of electrical parameters on various components of IGBT modules is suggested as approach for estimation of degradation in stressed devices. By comparison of these parameters for stressed and new components one can evaluate overall degradation of the module and find out the wear state of individual components. This knowledge can be applied for preventing early failures and for optimization of device design. The method is presented by regarding a standard type power module subjected to power cycling.**

I. Introduction

POWER devices are currently used in a wide range of applications including the automotive industry, wind and solar power energetics etc. In these diverse fields of application device design and construction do not always match the loads and as a result power modules can fail earlier than expected. Therefore, the interest in understanding and modelling the processes limiting the performance of a component is strong.[1], [2]

Obtaining the details regarding a mechanism responsible for a failure of a power electronic component is often problematic. Normally, a component is not investigated until it fails, and at this stage the information regarding the responsible mechanisms is lost due to catastrophic final stages of the failure leading for instance to burning of some parts, explosions or similar.[3], [4], [5], [6]. Especially the evolution and the distribution of the degradation processes causing the failure is difficult to assess afterwards. Therefore, many failure processes have been grouped into the same category even though they are very different with respect to dependence on the load. One of the possible approaches to solve this problem is to monitor on-state properties[7] of the device or its particular component and apply different types of investigation. This could be characterization through micro-sectioning[8] or focused ion beam (FIB) technique[4], [9]. However, as many failures occur after many years of operation at normal load a typical approach is to use accelerated tests in which high loads are applied. Under these conditions degradation occurs faster but one needs to be careful about failure mechanisms which could be not necessarily the same as for normal loads.

Electrical properties of power modules are governed by the quality of used materials and made interfaces or interconnections and, therefore, a subject of their degradation under the load. For example, the partly delamination of a bond wire will change the local current distribution as well as the effective resistance of the given interface. However, an eventual failure might constitute several types of subcomponent failures which is not necessarily measurable when considering a full module. One example of this is thermal fatigue. A power module is composed of several semiconductor chips, interfaces, and solders. Each of these might be damaged by temperature cycling and contribute to an eventual device failure. However, even if some individual components show significant wear the full module might still work due to the quite a number of elements constituting it[5], [9], [10], [11]. One of the ways to evaluate thermal-related degradation is to measure electrical properties of the components or interconnections individually.

Four-point probing or four-terminal sensing provides a high resolution technique for measuring local electrical properties of a given sample[9], [12]. By comparing the parameters measured for stressed and new components or interfaces one could assess the present quality state. Furthermore, in contrast to micro-sectioning or FIB, four-point probing is a non-damaging technique which renders it possible to use the sample after the analysis.

In the current paper, a four-point probing technique is developed for electrical measurements on individual semiconductor chips and interconnections: bond wires, solders, and metallizations in insulated gate bipolar transistor (IGBT) based power modules. This approach allows to assess the degradation type, speed, and distribution through different components as a function of stresses and time. It gives insights into understanding of failure mechanisms, as well as helps to optimize the module design. To illustrate the method standard IGBT modules subjected to power cycling are studied.

II. Method

A. Wire Geometry

The considered module consists of 6 identical sections designed as depicted in Fig. 1. Sections are numbered from one to six (S_1-S_6). This is merely a means of keeping an overview of the various sections.

Every section consists of two IGBTs (I_1 and I_2) and two diodes (D_1 and D_2). The IGBTs are connected to a DCB through a solder layer and 12 bond wires (w_1-w_{12}). In the same way the diodes are connected to the DCB with 16 wires. 16 wires on top of the diodes are placed uniformly and they have equal length, while 12 wires on top of the IGBTs are placed in varying positions and they are of varying lengths. From this point and forward we are separating the IGBT wires into four groups based on wire placement and length, which

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are presented in Table I.

TABLE I
GROUPING OF IGBT WIRES.

Wire #	Description
$w_{1,6,7,12}$	Longest wires placed at the edge of the transistors.
$w_{2,5,8,11}$	Shortest wires.
$w_{3,9}$	Medium length mid chip placed wires.
$w_{4,10}$	Almost same length as the first group and mid chip placed wires.

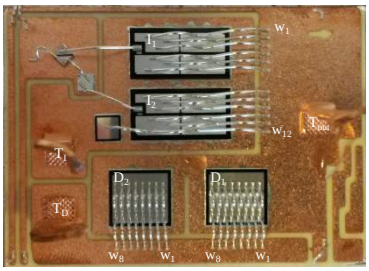

Fig. 1. Image of a single section of the power module under the study.

B. Power Cycling

In real life operation modules can fail earlier compared to the expected lifetime. The failure is typically catastrophic and any post failure analysis is complicated due to significant damage (in some cases even explosion) of the module. To investigate the reason for the failure the module needs to be removed from the load prior to it which is hardly possible. A widely used alternative way is to run so-called accelerated tests in which the modules are power cycled at some particular conditions and one can easy investigate the module with given number of cycles i.e. at the beginning, around the middle or close to the end of lifetime. Presently three modules are investigated: a new module for referencing, one close to failure (end of lifetime), and one in between (with respect to number of cycles). The samples are denoted module A, C, and B, respectively. The modules were power cycled with the current periodically ramped from zero to $300A$ as can be seen in Fig. 2. In power modules subjected to high pulsed currents or high frequency switching this is a commonly experienced load. [2], [7], [13]

In the test setup the module is mounted on a heatsink which is water cooled at a temperature below $40°C$.

C. Four-point Probing Setup and Procedure

The concept of four-point probing has been widely used for years. Originally, it was mainly applied semiconductor materials to measure the resistivity of, for example, transistors[12]. In the last years four-point probing became

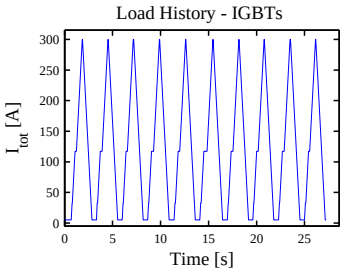

Fig. 2. Current load applied to transistor part of the module for a selected time frame.

a widely used method for different materials and various purposes. For instance, it was recently applied to estimate fracturing and degradation of materials through the change of resistance [9].

Sketch of our setup is presented in Fig. 3. We developed

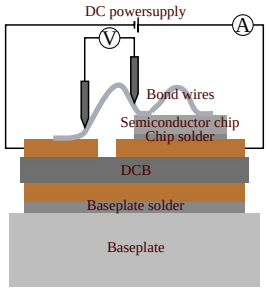

Fig. 3. Illustration of the four-point probing measurement method on a single wire of IGBT module.

a system providing positioning of the probes with very high precision on the micrometer scale. This allows us to repeat the measurement geometry on different parts of the device, i.e. to easily compare interfaces or interconnections of the same type. The idea of the method is to separate the probes supplying the current from the voltage measuring probes. This separation limits the current going through the probes measuring voltage thus minimizing the influence of the probe and contact resistances. It means that very small changes of resistance due to degradation of material or interfaces caused by thermal fatigue, delamination, lift-off etc. can be measured.

Depending on the position of the probes the expected signal varies. If measured across a semiconductor device, a non-linear relation is to be expected whereas everywhere else a strictly ohmic behaviour should be seen.

Using the above-described setup different configurations for probing are possible. Three approaches utilized in this work are described below.

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1) Sections: Potential difference as a function of applied current from terminal to terminal. As indicated in Fig. 1 three terminals are present: IGBT side (T_I), diode side (T_D), and the output terminal (T_{out}). Accordingly, the probing is divided into two measurements: $T_I \rightarrow T_{out}$ through the IGBTs and $T_{out} \rightarrow T_D$ through the diodes. By comparing results with a new module this gives an overall image of the section state including the semiconductor components, solder, metallization, and wires.
2) Chips: Potential difference across the four semiconductor chips as a function of applied current. The potential is measured locally on the chip surfaces meaning $T_I \rightarrow I_{1,2}$ and $T_{out} \rightarrow D_{1,2}$. This includes the state of the solder and metallization as well. The measurement is carried out at several selected positions on top of the chips.
3) Wires: Change in resistance of the wire/chip interfaces compared to a new sample of the same type. Initially the potential difference is measured on top of the wire curve, see Fig. 3. This is done with a fixed and known distance between the probes, thus making it possible to derive the local wire current. After obtaining the current distribution between the wires the potential difference between the probe positioned on the chip surface and one on the wire is measured. The local wire current together with the potential across the wire/chip interfaces yields an effective resistance. This resistance includes the wire itself, the bonded interfaces, and a small fraction of metallization/Cu beside the interfaces.

All measurements are performed using steady-state DC between 0-5 A. These are low currents for power modules. The reason for keeping the current low is to limit electro-thermal heating. However, even at these currents a local temperature change is found. Therefore, the temperature is controlled using Peltier elements and a PID concept i.e. applying a pause in between measurements and requiring a temperature variation below $0.1K$. The pause is also required to take into account the responsivity of the thermocouple, which is attached to the ceramic near the edge of the section.

Standard digital controlled power supplies are used for applying the current to the sample, the Peltier elements and for controlling the IGBT gates. For measuring the sample temperature and potential difference during probing high resolution multimeters are utilized.

For investigating the standard deviation of the method, measurements are repeated and compared to a reference. It is found that the voltage drop for ohmic measurements is reproducible within the μV interval. Furthermore, to continuously ensure the validity of the results a few selected approaches are utilized. The probing of the semiconductor components is carried out in several selected locations on top of the chip to ensure that the measured values are not local deviations. For wire measurements the calculated local currents are summed and compared to the total applied current.

D. SEM and Optical Microscopy

To relate the change of electrical properties of the power cycled modules with particular failures or degradation of the components scanning electron microscopy (SEM) equipped by FIB technique and micro-sectioning approach based on optical microscopy were used. SEM/FIB is primarily used to investigate the state of the metallization. The SEM/FIB analysis was carried out utilizing a Zeiss 1540 XB instrument. Due to limitations on the FIB milling range the wire interfaces were analysed using micro-sectioning. By combining mechanical cutting and micro particle polishing cross-sections of wire/chip interfaces are obtained and studied by optical microscope. The method and equipment are described in detail in [8].

III. Results

A. Four-Point Probing

Measurements across all interfaces of interest (method numbered 1 in II-C) were carried out on selected sections of the new module (A) and the most stressed module (C). This study showed that the voltage drop was much more significant on the IGBT chips compared to diodes. Accordingly, the full investigation was limited to the IGBT. Some measurements on diodes were carried out to provide comparison to IGBTs.

1) Sections: In Fig. 4 the electrical potential difference between terminals T_I and T_{out} (across IGBTs) as a function of the applied current is presented. The data are averaged on 5 sections for every module. In all three curves deviations obtained on different sections are included as errorbars.

From Fig. 4 the voltage drop is clearly seen to increase

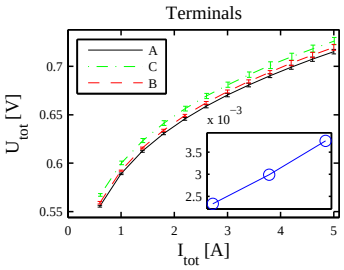

Fig. 4. Mean value of the potential difference between terminals plotted against the applied current with errorbars indicating the spread between the sections. The insert illustrates the voltage spread for three modules at $5A$.

with the number of cycles, indicating that the effective resistances of the sections are increased. This shows that the sections degrade over time when power cycled, as would be expected. One can also see that standard deviations are larger for C compared to A and B indicating that degradation is not evenly distributed among the sections. This is illustrated in the insert of Figure 4 where the voltage spread is plotted for the three modules. The potential differences from T_{out} to T_D (across diodes) were all found to be within the errors measured for module A.

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2) Terminal to Chip Surface: The measurement presented in Fig. 4 were repeated with the second probe placed on the surface of the chip metallization leaving out the bond wires. To rule out singular effects the probe was placed on several distinguishable positions on the metallization (corners, wire toes, center). All measurements showed change in voltage within the spread typical for module A. Therefore, it becomes obvious that the voltage change presented in Fig. 4 is related to degradation of the bond wire interfaces.

3) Wires - Current Distribution: In Figs. 5 and 6 the local current in the individual wires is presented as a function of the applied total current for two different IGBTs and diodes.

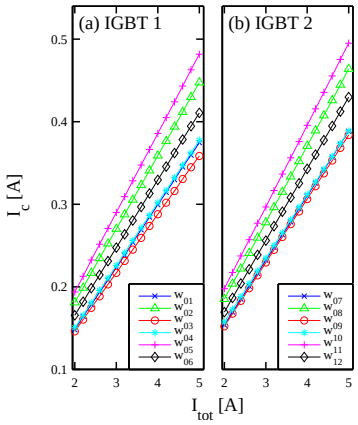

Fig. 5. Local current in each of the wires of a section from module A plotted against the total current.

In Fig. 5 a clear difference between the wires can be found. A good correlation between the wires geometry presented in Table I and dependences of Fig. 5 is observed. The shortest wires (namely, 2, 5, 8, 11) from the second group of Table I carry the highest current. The current in other wires follows well the geometrical placement and length. The deviation of the sum of the local currents in Fig. 5 is less than 5% compared to the applied total current. The results presented in Fig. 5 are for a single section, but qualitatively similar dependences are obtained for other sections of the same module as well as for the sections of modules B and C, i.e. those under given number of power cycles.

Compared to the current distribution between the wires on the IGBTs the current distribution between the wires of the diodes shown in Fig. 6 is much lower. Since all the wires on the diode chips are of the same length and geometry, the small differences between wires are credited to the random production deviations and chip edge effects.

4) Wires - Resistance: By using the calculated local currents and measured potential difference of each wire, an effective wire resistance is obtained. For samples C-S_3 and B-S_3 (where B and C are the modules and S3 is section number 3) these data are presented in Fig. 7 along with the mean values of resistance calculated for five sections of module A. From Fig. 7 it is clear that the resistances of the wires in samples B-S_3 and C-S_3 are higher than in the new module. The same tendency is found for the majority of the inspected sections.

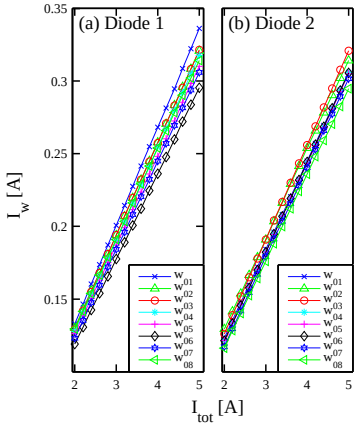

Fig. 6. Local current in each of the wires of a section from module A plotted against the total current.

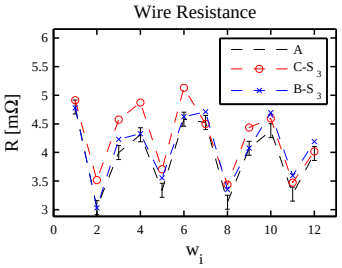

Fig. 7. Resistance of the IGBT bond wires for the selected section of modules B and C and averaged for module A. The lines between the values for different wires are presented only for visual guidance.

To better visualize the change in wire resistance between the cycled and new modules, the differences between the values measured on module C and A are presented for every wire and 3 different sections in Fig. 8. It is clear tendency that the wires at the edges of the sections (w_1 and w_{12}) are less degraded compared to those located in the middle of the section.

To obtain an overall picture of the wire degradation, mean values of resistance measured for each wire on 5 sections for every module are presented in Figs. 9 and 10. These figures show how the resistance varies for every wire from section to

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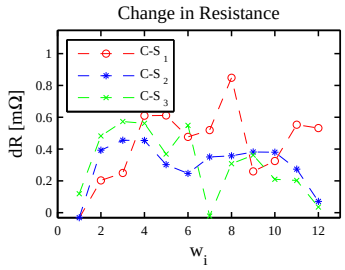

Fig. 8. Difference of resistance of the IGBT bond wires for 3 sections of module C compared to same wires of module A. The lines between the values for different wires are presented only for visual guidance.

section, i.e. gives the spread of resistance. From the figures

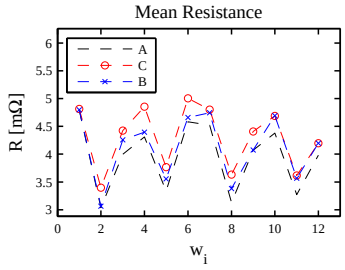

Fig. 9. Mean values of resistance obtained for each wire on 5 sections for every module A, B and C. The lines between the values for different wires are presented only for visual guidance.

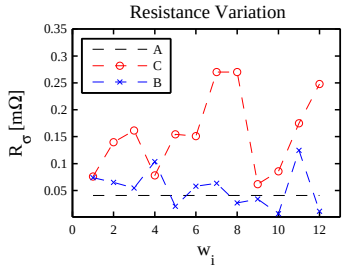

Fig. 10. Values for spread of resistance for every wire on 5 different sections for modules A, B and C. Dashed line corresponds to level of standard deviation for new module. The lines between the values for different wires are presented only for visual guidance.

it is obvious that both the resistance and its spread increase with number of cycles. Moreover, certain wires degrade higher than others. In the majority of samples large resistance changes are observed for the wires having shorter length and located either close to the middle of the chip or at the edge which neighbouring to the next IGBT chip. The very high spread seen for $w_{7,8,11,12}$ is generated by wires partly lifted off in one of the sections (as found by visual observation).

B. Microscopy Based Failure Mapping

It is found by four-point probing that resistance of wire interfaces increases that probably correspond to degradation under power cycling. However, different types of interfaces (wire bonds, metallization and solder) contribute to this degradation not in equal manner. To clarify the role of a particular interface it is important to carry out micro-analysis.

1) SEM and FIB: In Figs. 11a-d SEM surface images of the metallization of IGBTs and diodes for modules A and C are presented. In Fig. 11a the ordinary IGBT trench gate structure is clearly seen in the metallization. This is not the case for module C in Fig. 11b, here the surface is degraded and reconstructed. In contrast, no notable changes are observed for the diode metallizations as one can see in panels (c) and (d). These findings are in good agreement with the four-point probing measurements showing large spreads of local currents on IGBTs compared to the diodes.

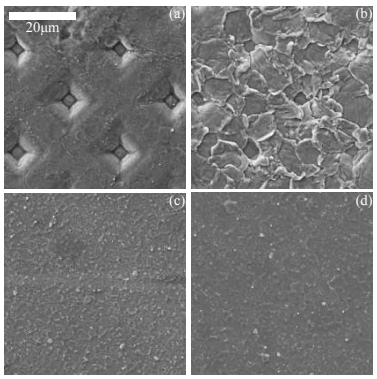

Fig. 11. SEM images of the chip metallization of the IGBT chips in module A (a), C (b), and the equivalent diode chips (c and d).

The reconstruction observed in the metallization is a well-known degradation process originated by thermal cycling, see [9], [10]. Reconstruction affects the forward voltage of the section if the metallization is: loosing contact to transistor channels, becoming thinner or causing wire delamination or lift-off. To validate the state of the entire metallization layer (not only surface) FIB milling was applied to obtain cross-sectional views. An example is presented in Fig. 12. It is found that only the surface layer of the metallization is reconstructed but the rest is in appropriate conditions. Minor diffusion of Si was found using elemental analysis.

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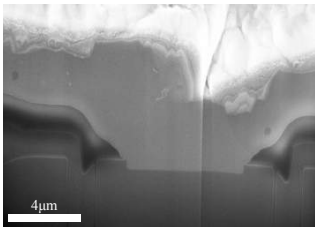

Fig. 12. SEM image of cross-section of the IGBT metallization from module C.

2) Micro-Sectioning: In Figs. 13 and 14 cross-sectional views of a bond wire interface are presented. They are obtained using micro-sectioning combined with optical microscopy. The interface corresponds to the end bond of C-S_1-w_3.

In Figs. 13 and 14 fractures propagating from both edges

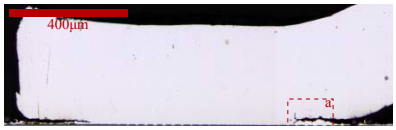

Fig. 13. Optical microscopy image of a wire/IGBT interface on section 3 of module C.

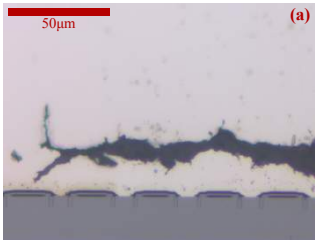

Fig. 14. Magnified part of the image presented in Fig. 13 as dashed rectangle.

of the bond more than $150\mu m$ inwards can be observed. At the heel of the end bond the fracture reaches ca. $50\mu m$ above the chip/metallization interface. From earlier studies it is know that this fracture development goes through the area in the wire which correspond to gradual interface between the refinement and deformation regions, see [4], [14].

IV. Discussion

A. Section State

By measuring the electrical potential difference across individual sections of stressed modules it was possible to establish the type of failure present. As seen in Fig. 4 the I-V dependences for IGBTs are non-linear. However, the increase of voltage from module A to B and further to C has linear dependence, i.e. corresponds to ohmic behaviour. The observed ohmic change indicates material fatigue, like mechanical creep of the solder or fracturing of the wire interface. Furthermore, by comparing the change in forward voltage for different sections of the same module, i.e. the spread presented in the insert, one can conclude that the power load is distributed unevenly through the sections because the spread increases. Fatigue is a fundamental occurrence in power cycled modules, however, unevenly distributed fatigue is undesired as the regions stressed additionally can cause early failures. For the diode chips the change of voltage for B and C modules was found to be within the standard deviations characteristic for the new module. Thus, one can conclude that there is no considerable degradation of diodes and related interfaces that is also confirmed by the microscopy investigations.

B. Diode Bond Wires

Four-point probing study of the diode bond wires showed very small difference in local currents from wire to wire as can be seen in Fig. 6. Assuming that the diode wires are (i) homogeneously placed on the chip surface, (ii) same length and (iii) are of the same quality of material it is very logical to suggest that they degrade in the same manner. From the SEM images of the metallization surface presented in Fig. 11 the state of the diodes reveal almost no restructuring that leads us to the conclusion of a low thermal load which is the main reason for degradation of metallization. The combination of the homogeneous current distribution and low load is assumed to be the primary reason for the diode interfaces to remain intact.

C. IGBT Bond Wires

In contrast to the bond wires on the diode chips, the IGBT wires are of unequal length and positioned differently on the chip. The current distributions presented in Fig. 7 show significant deviations from wire to wire. These deviations follow pretty well the geometrical layout of the wires. However, this type of design becomes problematic because local increase of current leads to additional thermal heating and thereby causes higher mechanical stress. From the data presented in Fig. 8 one can see that wires located at edges, namely, w_1 and w_{12} show the smallest change in resistance while those close to the central part of the chip demonstrate higher change. Near the outer edges of IGBTs a smaller change in temperature as well as a lower medium temperature are normally experienced during power cycling[5], [15]. The reason that $w_{6,7}$ do not show the same low damage as $w_{1,12}$ is the close proximity of the two chips which create a local heat-up in between the chips as well. The local stress might in the end create the basis for an early failure because lift-off of one of the wires place additional load on the surrounding wires.

The change observed in the effective wire resistance is primarily attributed to a change of the bond interfaces. The medium temperature and the current density is not deemed high enough to create significant material changes of the wire itself, e.g. through diffusion or electro-migration. However, the

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power cycling is expected to cause fatigue and fracturing due to mismatch in the expansion coefficients near the interfaces. This is supported by the micro-sectioning images of a wire interface in Figs. 13 and 14. Here the dominating degradation is clearly seen to be located around the refinement area of the wire. One can also suggest that the metallization reconstruction on the IGBT chips seen in Fig. 11 can assist the wire lift-off.

D. Degradation Evolution and Distribution

By considering the average change in resistance of a given wire interface together with the spread of resistance between various sections it is possible to map both the evolution and distribution of the damage. In Fig. 9 the mean value of the resistance is clearly seen to increase with number of cycles. The spread between sections plotted in Fig. 10 can give an estimate of the design quality as well as production quality. If the module was ideally designed creating a homogeneously distributed load under operation, then the spread would remain close to that of a new module as the same type of wires would degrade identically. However, the large variation observed for different wires of module C allows to suggest that the degradation is centered around wires as well as selected sections.

V. Conclusion

Four-point probing method is used for measurements of electrical parameters of power modules. The μV resolution of the developed setup enables investigating the condition of the majority of elements, including various interfaces which are known to be primary origins for most of failures. The originality of the approach is in estimation of correlations between degradation of electrical parameters (for instance, resistance) and development of damages on the microscopic level which are monitored using optical or electron microscopy.

The method was employed on an IGBT module with a tendency of early failure at certain field loads. Modules at three different stages of lifetime were investigated, namely new module, module close to failure, and one in between. The load applied to the modules causes thermal cycling similar to that experienced by standard power converters in real operation.

The measurements on entire sections demonstrated the non-linear behaviour expected for semiconductor components. Modules B and C show considerable increase in forward voltage compared to the new module indicating material degradation. The difference between new and worn modules is observed to be of ohmic nature. This is an indication that the ageing and fatigue happens predominantly in interfaces and not in the semiconductor components. It is found that various sections of the same module degrade in different ways most probably due to the fact that the power load is not evenly distributed. Comparing data from different chips it was observed that IGBT's metallization and bond wires degrade significantly compared to those on diode chips. This degradation was assigned to difference in load and wire geometry on IGBTs. Difference in length and configuration of wires leads to increase of local currents on some of them. Higher local currents cause additional heating and mechanical stresses at the interfaces due to the difference in expansion coefficient for the metallization layer and chip. Moreover, restructuring of metallization is found which could serve as additional factor for fracturing and wire lift-off.

Good agreement between degradation of electrical parameters and formation of structural defects is established. Thus, the four-point probe measurements can be suggested as independent and relatively easy method for estimation of device quality, its ageing and fatigue under operation as well as for the control of production quality.

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References

[1] U.Scheuermann and U.Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," *PCIM Nuremberg*, p. 5964, 2002.

[2] W. Kanert, "Active cycling reliability of power devices: Expectations and limitations," *Microelectronics Reliability*, vol. 52, pp. 2336–2341, 2012.

[3] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test for igbt modules in traction application," *Proc. Power Electronics and Drive Systems*, pp. 425–430, 1997.

[4] J. Goehre, M. Schneider-Ramelov, U. Geissler, and K. Lang, "Interface degradation of al heavy wire bonds on power semiconductors during active power cycling measured by the shear test," in *CIPS*, no. 3.4, 2010.

[5] O. Schilling, M. Schfer, K. Mainka, M. Thoben, and F. Sauerland, "Power cycling testing and fe modelling focussed on al wire bond fatigue in high power igbt modules," *Microelectronics Reliability*, vol. 52, pp. 2347–2352, 2012.

[6] R. Amro and J. Lutz, "Power cycling with high temperature swing of discrete components based on different technologies," in *IEEE Power Electronics Specialists Conference 2004*, 2004, pp. 2593–2598.

[7] P. Ghimire, K. B. Pedersen, A. R. de Vega, B. Rannestad, S. Munk-Nielsen, and P. Thgersen, "A real time measurement of junction temperature variation in high power igbt modules for wind power converter application," in *8th International Conference on Integrated Power Electronic Systems*, 2014.

[8] K. Pedersen, P. Kristensen, V. Popok, and K. Pedersen, "Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in igbt modules," *Microelectronics Reliability*, vol. 53, pp. 1422–1426, 2013.

[9] S. Pietranico, S. Lefebvre, S. Pommier, M. Bouaroudj, and S. Bontemps, "A study of the effect of degradation of the aluminium metallization layer in the case of power semiconductor devices," *Microelectronics Reliability*, vol. 51, pp. 1824–1829, 2011.

[10] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, pp. 653–667, 2002.

[11] H. Ye, M. Lin, and C. Basaran, "Failure modes and fem analysis of power electronic packaging," *Finite Elements in Analysis and Design*, vol. 38, p. 601612, 2002.

[12] L. Valdes, "Resistivity measurements on germanium for transistors," *Proceedings of the IRE*, pp. 420–427, 1954.

[13] J. Lutz, U. Scheuermann, H. Schlangenotto, and R. Doncker, *Semiconductor Power Devices - Physcis, Characteristics, Reliability*. Springer-Verlag, 2011.

[14] K. Pedersen, P. Kristensen, V. Popok, and K. Pedersen, "Interface structure and strength of ultrasonically wedge bonded heavy aluminium wires in si-based power modules," 2014, to be published.

[15] B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, and M. Thoben, "Thermo-mechanical analysis of bonding wires in igbt modules under operating conditions," *Microelectronics Reliability*, vol. 52, pp. 2353–2357, 2012.

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PAPER D

A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application

A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application

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Abstract

This paper presents a real time measurement of on-state forward voltage and estimating the junction temperature for a high power IGBT module during a power converter operation. The power converter is realized as it can be used for a wind turbine system. The peak of the junction temperature is decreased at higher fundamental frequency due to change in on-state time from the change in output frequency. The junction temperature is estimated using the on-state collector-emitter voltage of the IGBT module. Lower output frequency is thermally a higher stressing zone for wind power converters, hence the low frequency range is considered from 6Hz to 20Hz; the corresponding on-state collector-emitter voltage and junction temperature are presented. The estimation of junction temperature is compared with finite element based thermal simulations. The peak temperatures at different frequencies are compared between measurement and simulation results. The measurement technique desinged to be implementable for field application.

1 Introduction

Wind turbine technology is growing rapidly since its instalment in 1980s [1]. Due to the intermittent nature of wind, grid code requirements and the high power density, the power electronic converters suffer mostly to fulfill reliability issues [2, 3].

Power transistors are expensive and most vulnerable part in wind power converters for higher oscillating junction temperature. Silicon based multichip Insulated Gate Bipolar Transistor (IGBT) power modules are mostly in use, which have weak capability against high amplitude thermal cycle. In fact, the hardness of the silicon causes the failures due to higher thermo-mechanical stress [4]. Generally, solder degradation and bond wire lift-off are the major failures in multi-layer modules [5]. A number of IGBTs are mounted in one converter depending upon the converter topology [2]. A survey conducted on offshore wind turbine technology shows that power modules are the most vulnerable part in their electrical system [6, 7].

In comparison to traction application, a real time monitoring is more rare in wind power converters [8]. In order to avoid the catastrophic failure of the device and to improve the total reliability of power converters, an online monitoring method may play a vital role in power converters. In regards to IGBTs, the major electrical-thermal parameter such as thermal impedance, gate threshold voltage, gate capacitance, collector emitter voltage etc. are considered as ageing parameters [5, 9-10]. A deviation in those parameters such as 10-20% increment on V_{ce}, may be used as failure criteria for the transistor [11]. Out of those parameters, a temperature sensitive parameter (TSEP) which in this case is the on-state collector- emitter voltage (V_{ce}): is used to estimate the junction temperature of the IGBT while the converter is in operation [12].

This paper presents a method to measure the on-state V_{ce} while the converter is in operation. In order to realize a real life application, a wind power converter is used and the measurement is conducted at lower frequency range from 6Hz to 20Hz. Operating at lower frequency range increases thermal stress to the power module due to power losses over longer time period. Especially, in case of a doubly-fed induction generator (DFIG), the inverter has to deliver excitation energy at a frequency from 0Hz to 16Hz [8]. The converter is thermally stressed and has proven the weakest part in terms of reliability for wind power converters. Therefore, a focus is given in the thermal stressing zone.

2 IGBT power module

The power module consists of multi-layers of different packaging materials with unmatched coefficient of thermal expansion (CTE). The junction temperature monitoring is important because the major failures such as bond wire fatigue, solder joint fatigue etc. are dependent on thermal loading such as temperature swing, mean temperature and electrical parameters. [11].

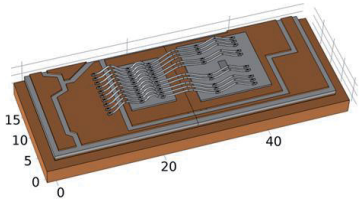

Figure 1 CAD figure showing one section of a module. The section consists of one IGBT chip, one diode chip and 10 bond wires.

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A 1700V/1000A IGBT power module is used as a device under test module. The module consists of identical sections each with two IGBT chips, two diodes, and 20 bond wires. Apart from this it is an ordinary direct copper bonded (DCB) substrate with an *AlN* ceramic, large *Al* wires, and a *Cu* baseplate. The geometry is depicted in Figure 1 and the thickness of the various layers is seen in Table 1.

Material	Thickness [µm]
Bond wire – *Al*	400
Metallization – *Al*	3
Chip – Diode/IGBT	300
Die attach – solder paste	50
Copper	300
Ceramic -*AlN*	700
Copper	300
DCB attach - Solder paste	100
Baseplate – *Cu*	3000

Table 1 Vertical layers of the IGBT module with layer, thickness and composition

3 Power converter

An H-bridge topology is used as a converter where half bridge IGBT modules are used on each leg as depicted in Figure 2 [13]. One leg is used as a device under test (DUT) and the other is used as a control side in order to control the power flow. In the control side, two legs are used to share the current from the DUT. This ensures the IGBT modules of the control side to not wear-out prior to the DUT.

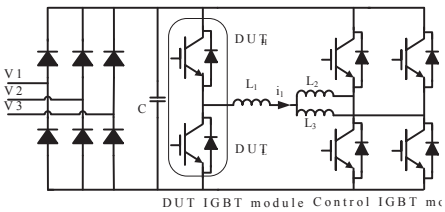

Figure 2 A power converter topology

Where,
DUT_H: High side of device under test IGBT module
DUT_L: Low side of device under test IGBT module
L_1, L_2, L_3: Load inductors

The power converter operating parameters are shown in Table 2.

Parameter	Value
DC link voltage (V_{DC})	1000V
Outpput voltage (V_{out})	315Vrms
Load current (I_L)	630Arms
Fundamental frequency(f_{out})	6Hz
Switching ferquency (f_{sw})	2.5kHz
Water temperature for cooling	80°C

Table 2 The converter operating electrical parameters

4 Measurement technique

As discussed before, an on-state V_{ce} is chosen as an ageing and temperature monitoring parameter. As the DC-link voltage is 1000V, so during switching period the collector-emitter voltage swings between less than 1V to 1.14KV due to transient loading as illustrated in Figure 3. Hence, the circuit should have featured with high blocking voltage with a very good accuracy.

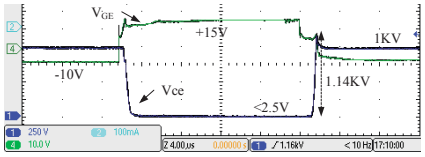

Figure 3 A V_{ce} turn on/off waveform and transient during switching

In addition to this, the on-state voltage has transient behaviour during turn-on time due to dynamics of the switching. Hence, the voltage measurement circuit should measure the voltage after completing the transient region as shown in Figure 4 to increase the accuracy of the measurement. Approximately, the on-state voltage has dynamics for the first 12µS in the tested IGBT module as illustrated in Figure 4.

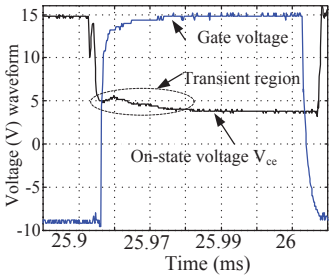

Figure 4 Gate emittter voltage waveform and V_{ce} voltage waveform measured at V_{b1}

4.1 Voltage measurement

The circuit is built to measure the on-state V_{ce} and V_{FD} during the converter operation. A single circuit is able to measure both high and low side IGBTs and diodes of the DUT. Details of the circuit are described by Szymon et al. [14]. The circuit is built to be operational in real life ap-

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plications. Figure 5 shows the measurement circuit used to measure the V_{ce}.

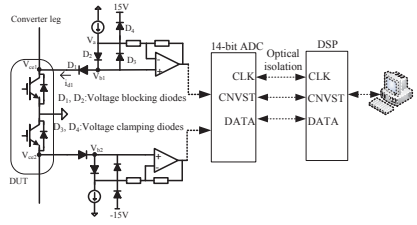

Figure 5 A V_{ce} measurementt circuit

Two diodes are connected in series and a weak current source is forward-biased them during IGBT turn-on time as given in Figure 5. When the IGBT is off, the diode D_1 is blocked the V_{ce} voltage.

$$V_{ce1} = V_{b1} - V_{D2} = V_{b1} - (V_a - V_{b1}) = 2V_{b1} - V_a \quad (1)$$

Assuming that the two diodes are identical V_{D1}=V_{D2}, the V_{ce} is measured by subtracting the voltage drop on D_2 from V_{b1} potential as given in Equation 1. V_{D1} and V_{D2} are voltage across D_1 and D_2 respectively. The measurement part of the circuit is isolated using an optical fibre connection with the rest of a data logging system.

5 Junction temperature estimation

Junction temperature monitoring is of a paramount interest to improve the total reliability of power converters. A calibration of V_{ce}-T_j is conducted to obtain a calibration factor at higher current levels in the converter itself. A time is taken in account to rise up the current and to fall at zero level during the calibration process. The coolant temperature is maintained at a constant value during the measurement process. Finally, the junction temperature is calculated based on the real time measurement of the on-state voltage and the calibration factor.

5.1 V_{ce}-T_j Calibration

Initially, the on-state V_{ce} and T_j are calibrated at temperatures ranging from 22°C to 80°C for up-to 960A_{peak}. The baseplate temperature is kept homogenously distributed by using Danfoss shower power [15] and by controlling the coolant temperature. A self-heating of the power converter is used to increase the coolant temperature.

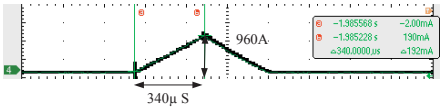

Figure 6 A current waveform during calibration

During the calibration process a normal PWM switching of the converter is turned off. The current i_1 is ramped up through the inductors and the respective current and on-state voltage for IGBTs and free-wheeling diodes are measured as shown in Figure 6.

Each calibration process takes 680µs at one temperature level. Figure 7 (a) shows the V_{ce}-T_j calibration and Figure 7 (b) shows a calibration factor for IGBT module at different current levels.

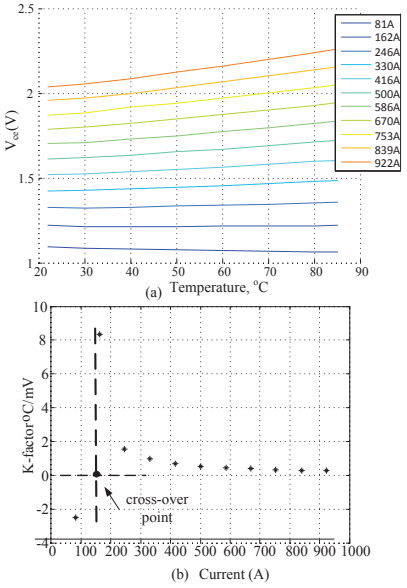

Figure 7 A Vce-Tj calibration (a) Vce-Tj calibration at diffrent current level (b) A calibration factor for IGBT

6 Thermal Simulation

The thermal modeling contains two interconnected problems, namely the power loss inside the module and the distribution of heat. The power loss and temperature problems are interconnected e.g. through the temperature dependence of physical parameters like the electric and thermal conductivity. But even more so through the complex non-homogeneous fields created inside power modules by transient loads [16-17].

In the following section a finite element method (FEM) is presented for the evaluation of the temperature field as a function of time. The derived results are compared to the temperature measured online. The model presented is based on the work carried out in [17], where everything is presented in detail. In the present only relevant data is included.

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6.1 Physical parameters

In modern FEM based simulations one of the governing factors are the physical parameters [18]. With regards to pure materials like the *Al* wires and the *Cu* pads this is a simple matter, however, the IGBTs and the diodes are in principal non-linear and non-isotropic structures which are not ideal for continuum assumptions. This is solved by using so-called effective medium parameters for the elements representing the semiconductor chips in the calculations. This is presented and discussed in detail in [19] and [17]. For all materials, temperature dependent parameters are introduced for vital coefficients like the thermal and electrical conductivity.

6.2 Power loss

The power loss inside the module may roughly be divided into conduction-, switching-, and gate loss: where the last one is normally neglected: [19]

$$P_{tot} = P_{cond} + P_{SW} + P_{gate} \approx P_{cond} + P_{SW} \quad (2)$$

The conduction loss is an ordinary ohmic contribution which affects all current carrying components of the geometry in Figure 1, namely the DCB, wires, chips, and solders.

6.2.1 Conduction Loss

All contributions from the conducting metals of the geometry are considered evenly distributed and are calculated from the electrical conductivity of pure materials. The semiconductors on the other hand are more complicated as discussed in the previous section as these are non-isotropic, non-linear materials. The IGBTs consists of a large amount of parallel transistor channels, which ideally are identical. In a similar way the diode acts as a channel as well. All conducting channels of the semiconductors are assumed to perform evenly, and the only changes in the current distribution allowed are created by the temperature fields. Apart from that the power loss is calculated based on datasheet specifications.

6.2.2 Switching Loss

The switching loss is a phenomenon only observed in the semiconductor chips. In the IGBT, the switching loss includes the energy required to switch on and off the component, whereas in the diode only the so-called recovery loss is included [21].

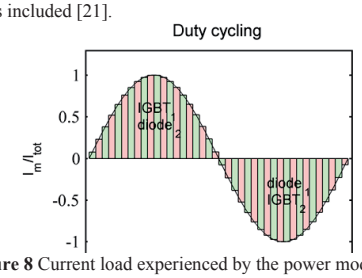

Figure 8 Current load experienced by the power module

In Figure 8, the duty cycle load applied to the module is illustrated. The current attains a sinusoidal waveform which accordingly yields the sinusoidal on-state voltage as shown in Figure 12. Each of the color bars in Figure 8 symbolize a switching period of time: $t_{sw} = t_{on} + t_{off}$. In Figure 9, the power loss in a single period for one IGBT chip is illustrated. As illustrated the switching loss is in principle placed initially and in the end of the period, when switched on and off respectively. In the present, the switching loss is assumed evenly distributed during the on-state time t_{on} and considered constant P_{swm} in the given on-state.

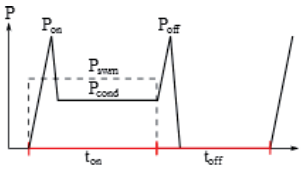

Figure 9 Power loss in a single IGBT chip during one switching cycle [20].

6.3 Thermal model and boundary conditions

The FEM simulation in principle only concerns solving the convection-diffusion-reaction problem as described in [16-17]. Solvers, meshing, and geometrical specifications are carried out and specified in COMSOL multiphysics. Therefore one of the primary assignments, as discussed in [16], is to specify the proper boundary conditions.

Baseplate cooling is one of the governing factors apart from the power loss. As mentioned in Section 5.1, the baseplate is water-cooled directly using Danfoss shower-power. Based on the pumping capacity as well as the mixture of water and glycol the convection coefficient h_{SP} can be obtained from [21], so that the normal heat flux out of the baseplate may be calculated as given in Equation (3):

$$q_n = h_{SP}[T_{water} - T(x, y)] \quad (3)$$

Here the water temperature is assumed constant across the baseplate and over time. This assumption is supported by measuring the cooling water temperature over time which is kept close to 80°C. From Figure 1, it is clear that only a reduced geometry is considered. Out of the six sections only half a section is regarded. This means that interactions between individual sections and the two halves of a section need to be included in the boundary conditions. The former is assumed to only affect the medium temperature of the section as the primary power is dispersed towards the backside of the baseplate. This is accounted for through fitting to the experimental data. The latter interaction, however, is more complicated. As the missing part of the section is an inverted mirror of the part illustrated the total power passing through the plane separating them will be the same. The flux field, however, will be inverted in the same way as the geometry. This is included simply by adding the outgoing flux from the IGBT and the diode

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respectively as an ingoing flux half a period later with a correction with respect to the inversion. The remaining boundary conditions are kept simple to speed up calculations. This means that the silicone gel covering the components is treated as a passive convection surface. And all inside connections are assumed ideal.

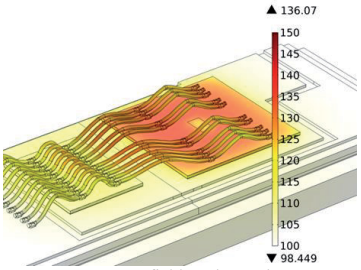

Figure 10 Temperature field at the peak IGBT temperature at an output frequency of 6Hz

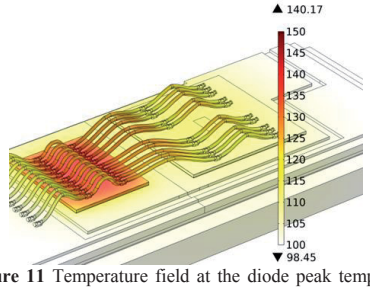

Figure 11 Temperature field at the diode peak temperature at an output frequency of 6Hz

6.4 Temperature curves

The used conditions for the simulations are the same as listed in Table 1. With the mentioned conditions for the simulations 30 cycles had to be computed before reaching the equilibrium period. With respect to resolution of meshes and time stepping it was refined until conversion of the final result. In Figure 10 and 11, the surface temperature field of the diode and IGBT chips are presented at their peak values. The simulation is carried out at a 6Hz output frequency. As would be expected the temperature is significantly higher in the center of the chips and decreases towards the edges. This illustrate one of the difficulties of working with online measuring of the temperature as the peak value differs significantly from the mean junction temperature, as illustrated in Figure 14.

7 Measurement and simulation results

The online measurement is conducted from 6Hz to 20Hz on every 2Hz increment. The on-state V_{ce} and V_{FD} are measured for the high side and low side IGBTs and diodes respectively as shown in Figure 12.

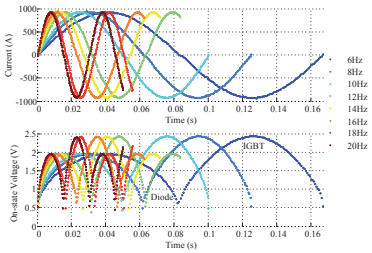

Figure 12 A measured on-state Vce from 6Hz to 20Hz for IGBTs and diodes

The on-state voltage when the current at 920A is compared and found that the V_{ce} is closely 10mV less in low side IGBT at 20Hz than the 6Hz frequency. The junction temperature is calculated for different frequencies as shown in Figure 13.

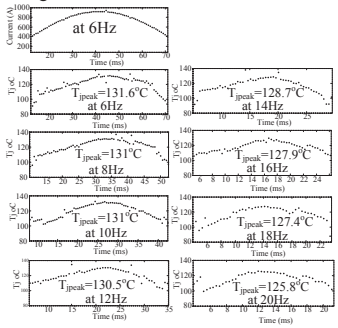

Figure 13 A measured peak temperature variation at different frequency

The peak temperature variation for IGBTs at 6Hz to 20Hz frequencies are shown in Figure 14 for measured and thermal simulated results. As seen in the figure, it is clear that both results fairly match the peak and temperature variation on each half cycle.

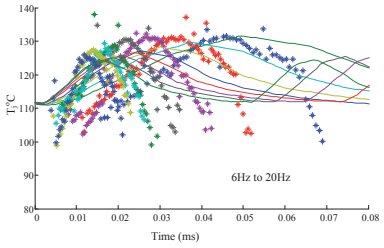

Figure 14 A T_j variation in measured and simulation compared together for 6Hz to 20Hz

To illustrate more in comparison between two studies, only peak temperature variations on each frequency are plotted in Figure 15. The peak temperatures T_j are very

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close. In conclusion, the peak junction temperature drops 131.6 to 125.8 which is 5.8°C from 6Hz to 20Hz in the measurement.

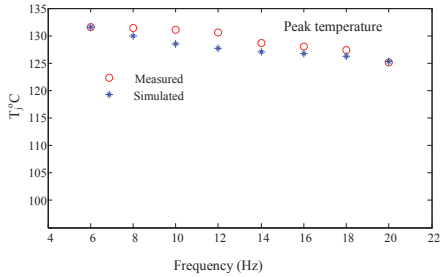

Figure 15 A comparison of peak T_j between measured and simulation

8 Conclusion

The junction temperature is monitored in real time while a power converter is in operation and the peak temperature is increased by approximately 5.8°C from 20Hz to 6Hz application for a 1700V and 1000A module. The thermal analysis using FEM simulation is conducted and peak temperature variation fairly matches between measurement and simulated results. This measurement technique is less complex and easy to implement in field application.

Acknowledgement

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9 References

[1] Liserre, M.; Cardenas, R.; Molinas, M.; Rodriguez, J.: Overview of multi-MW wind turbines and wind parks. Industrial Electronics, IEEE Transactions on. Vol. 58, no. 4, pp. 1081-1095, 2011.

[2] Blaabjerg, F.; Liserre, M.; Ke, M.: Power electronics converters for wind turbine systems. Industry Applications, IEEE Transactions on. Vol. 48, no. 2, pp. 708-719, 2012.

[3] Chen, Z.; Guerrero, J.M.; Blaabjerg, F.: A review of the state of the art of power electronics for wind turbines. Power Electronics, IEEE Transactions on. Vol. 24, no. 8, pp. 1859-1875 2009.

[4] Pedersen, K.,B.; Pedersen, K.: Bond wire lift-off in IGBT modules due to thermomechanical induced stress. Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on. PP. 519-526, 2012.

[5] Ciappa, C.: Selected failure mechanisms of modern power modules. Microelectronics Reliability. Vol. 42, no. 4–5, pp. 653-667, 2002.

[6] Yang, S.; Bryant, A.; Mawby, P.; Xiang, D.; Ran, L.; Tavner, P.: An industry-based survey of reliability in power electronic converters. in Energy Conversion Congress and Exposition. ECCE 2009. IEEE. 2009, pp. 3151-3157.

[7] Song, Y.; Wang, B.: Survey on reliability of power electronic systems. Power Electronics, IEEE Transactions on. Vol. 28, no. 1, pp. 591-604 2013.

[8] Bartram, M.; Von Bloh, J.; De Doncker, R.W.: Doubly-fed-machines in wind-turbine systems: is this application limiting the lifetime of IGBT-frequency-converters? in Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual. 2004, pp. 2583-2587 Vol.4.

[9] Smet, V.; Forest, F.; Huselstein, J.-.; Richardeau, F.; Khatir, Z.; Lefebvre, S.; Berkani, M.: Ageing and failure modes of IGBT modules in high-temperature power cycling. Industrial Electronics, IEEE Transactions on. Vol. 58, no. 10, pp. 4931-4941 2011.

[10] Patil, N.; Celaya, J.; Das, D.; Goebel, K.; Pecht, M.: Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics. Reliability, IEEE Transactions on. Vol. 58, no. 2, pp. 271-276 2009.

[11] Ghimire, P.; Beczkowski, S.; Munk-Nielsen, S.; Rannestad, B.; Thogersen, P.B.: A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT. EPE'13 ECCE Europe 15th European Conference on Power Electronics and Applications, Lille, France. Sep. 2013. In press.

[12] Schmidt, R.; Scheuermann, U.: Using the chip as a temperature sensor — The influence of steep lateral temperature gradients on the Vce(T)-measurement. in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on. 2009, pp. 1-9.

[13] R.O. Nielsen, J. Due and S. Munk-Nielsen, "Innovative measuring system for wear-out indication of high power IGBT modules," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 1785-1790.

[14] Beczkowski, S.; Ghimire, P.; de Vega, A.R.; Munk-Nielsen, S.; Rannested, B.; Thøgersen, P. B.: Online Vce measurement method for wear out monitoring of high power IGBT modules. EPE'13 ECCE Europe 15th European Conference on Power Electronics and Applications, Lille, France. Sep. 2013. In press.

[15] Olesn, K.; Bredtmann, R.; Eisele, R.:"ShowerPower" New Cooling Concept for Automotive Applications, 2006.

[16] Schilling, O.; Schfer, M.; Mainka, K..; Thoben, M.; Sauerland, F.: Microelectronics Reliability, vol. 52, pp 2347-2352, 2012.

[17] Pedersen, K.B.; Pedersen, K..: Dynamical Modelling Method of Electro-Thermo-Mechanical Fatiguee in IGBT Modules. To be published.

[18] Codina, R.: Computer Methods in Applied Mechanics and Engineering, vol. 156, pp 185-210, 1998.

[19] Filipis, S.; Kock, H.; Nelhiebel, M.; Kosel, V.; Decker, S.; Glavanovic, M.: Microelectronics Reliability, vol. 52, pp 2374-2379, 2012.

[20] Rajapakse, A.; Gole, A.; Wilson, P.: Approximate loss formulae for estimation of IGBT switching losses through emp type simulations, IEEE, 2005.

[21] Lutz, U.; Scheuermann, U.; Doncker, R.; Schlangenotto, R.: Semiconductor Power Devices – Physics, Characteristics, Reliability, Springer-Verlag, 2011.

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PAPER E

Real time wear-out monitoring test setup for high power IGBT modules under sinusoidal loading condition

Real time wear out monitoring test setup for high power IGBT modules

Pramod Ghimire, Kristian Bonderup Pedersen, Bjørn Rannestad, Stig Munk-Nielsen, Paul Bach Thøgersen, and Peter de Place Rimmen

***Abstract*—This paper presents a real time wear out monitoring test setup and experimental study of ageing in high power IGBT modules under sinusoidal loading conditions. Online monitoring of on-state forward voltage on each individual device of half bridge modules are presented in converter operation. Data evaluation theory separating wire degradation and solder degradation is presented. Four power modules are tested at $6Hz$ output frequency, under sinusoidal loading with $922A$ peak at $80°C$ cooling liquid for different number of cycles. Through mapping of the degradation as a function of number of cycles the identification of the failure source is enabled. The proposed test setup is robust, reliable and safe to conduct both destructive and non destructive tests for reliability studies. Preliminary post test investigations are included to identify degradation mechanisms that could be a source for a change in electrical parameters.**

***Index Terms*—IGBT power module, on-state forward voltage, thermal responsivity, power module degradation, active thermal cycling, power electronics reliability, real time monitoring, wear out monitoring**

I. Introduction

In modern high power applications health monitoring of power modules are capturing interests to improve reliability. During real life operation power converters suffer from internal and external overloads during a lifetime. Internal overloads originate from: electrical and mechanical connections, under-voltage/over-voltage, etc. Similarly, external overloads originate from: lightning, temperature gradients, humidity, air pollution, vibration, etc. [1]. In spite of these stressors, power converters still need to satisfy grid code requirements [2].

Two types of accelerated tests are normally used: active thermal cycling/power cycling (A-TC) and passive thermal cycling (P-TC). A-TC is a common approach for evaluating design and performance under a given loading, as well as end of life tests at accelerated conditions [3], [4], [5], [6], [7]. In A-TC setups the device under test (DUT) is normally heated through sheer conduction losses. However, to get closer to real world stresses the DUT is in this setup handled as an active component and switched under normal conditions. Accordingly, switching losses constitute a significant part of the total power loss. The proposed test method is categorised as an advanced A-TC method as demonstrated in Fig. 1. Conventional A-TC is carried out to study mainly degradation of bond wires and solder joints under a pulsating current.

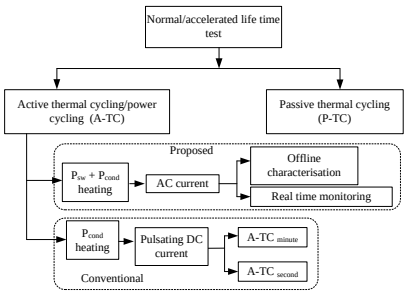

Fig. 1. Proposed test in context with conventional test methods.

Test procedure and working conditions for different failure mechanisms in conventional components are well defined in standards and literature [8], [9], [10]. Mainly three electrical and thermal parameters are found sensitive to the wear of power modules: on-state υ_{ce}, gate threshold voltage ($V_{ge,th}$), and thermal resistance (R_{th}) [11], [12]. These parameters are also identified as possible sources of a well defined failure criteria. Here real-time monitoring of υ_{ce} as an ageing indicator of the interconnections is proposed through a real time monitoring of those parameters in real application [13], [11], [14].

This paper proposes a method to measure change in the thermal resistance during steady state sinusoidal loading of a converter. By monitoring the parameters a clear image of component degradation is obtained continuous in real time. This method not only helps identify possible failure mechanisms but also improving lifetime modelling approaches of power modules afterwards. Four power modules are tested with similar loading parameters for all components of each device; such as high side IGBT ($I_{DUT,H}$), corresponding free-wheeling diode ($D_{DUT,H}$), low side IGBT ($I_{DUT,L}$), and corresponding free-wheeling diode ($D_{DUT,L}$). Finally, the tested modules are inspected after being removed from the test setup using scanning electron microscopy (SEM) and micro-sectioning [15].

II. Test Setup

One leg of a 3-phase wind power converter is simulated by applying a pulse width modulation (PWM) controlled continuous sinusoidal current as primary stress of the DUT. The setup consists of the DUT and a control side (CTRL) where the latter is split into two separate legs of two devices to ensure the DUT fails first. A block diagram of the setup is demonstrated in Fig. 2a together with a picture of the physical setup in Fig. 2b. One benefit of this setup is that while large magnitudes of power is circulated by the switches only losses of the system are to be supplied.

A. Power Converter

A circuit diagram of the power converter is shown in Fig. 3. Phase and magnitude of the two voltage sources V_{DUT} and V_{CTRL} are controlled by duty cycling each leg. In this test, DUT works as connected to generator side while CTRL works as connected to load side. Here the current peak of $922A$ at $6Hz$ frequency is controlled by adjusting V_{CTRL} and the voltage across the $380\mu H$ inductor from the CTRL leg. The equivalent inductance, as given in Eq. (1), is able to filter the current ripple because the effective pulse difference is

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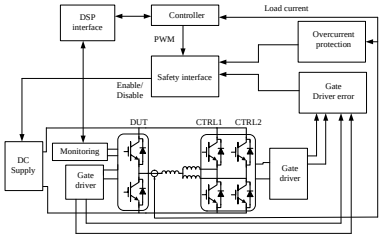


(a) Block diagram.

(b) Test setup.

Fig. 2. Block diagram layout and picture of the proposed test setup.

limited during switching of the legs. The parallel legs of the control side shares similar current at identical switching action, hence the voltages V_{CTRL1} and V_{CTRL2} are equal in phase and magnitude.

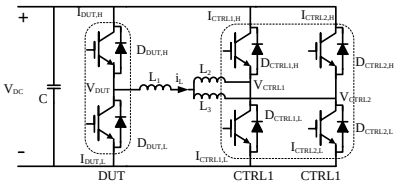


Fig. 3. Power converter topology.

$$L_{eqv} = L_1 + \frac{1}{2}(L_2 + L_3), \tag{1}$$

where L_{eqv} is an equivalent inductor including series inductor L_1 and two similar magnitude current sharing inductors L_2 and L_3. When i_L is positive, the six elements conducting are $I_{DUT,H}$, $I_{CTRL1,L}$, $I_{CTRL2,L}$, $D_{DUT,L}$, $D_{CTRL1,H}$ and $D_{CTRL2,H}$, where I and D denote the IGBT's and diodes, respectively. As the current i_L is out of phase with V_{DUT}, in this analysis the switching duty cycle will be less than 50% for the $I_{DUT,H}$ as well as for the control HS during positive half current cycle. Consequently, the $D_{DUT,L}$, $I_{CTRL1,L}$ and $I_{CTRL1,L}$ conducts a longer time. Similarly, for the negative half cycle additional stress appears on $D_{DUT,H}$, $I_{CTRL1,H}$ and $I_{CTRL1,H}$. In both cases the CTRL shares the total current, therefore the diodes on DUT are the mostly stressed components, with respect to the applied current.

The converter requires a power supply able to provide fluctuating power as well as maintaining the DC link voltage steadily at $1000V$. As demonstrated in Fig. 4, this is achieved through a frequency converter in order to ensure the steady DC voltage. A $100Hz$ step up transformer with a gain of 2.2 is used prior to rectify the grid voltage to allow maximum of $1188V$ on DC side. This is also sufficient to compensate the voltage drop in series inductances and resistances.

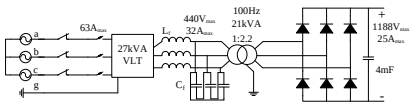


Fig. 4. DC power supply.

B. Controller

The DUT leg has an open loop space vector modulated (SVM) voltage (V_{DUT}), while the control side of converter has close loop control in order to force a sinusoidal current through the devices. In this measurement, the phase displacement (ϕ) of V_{DUT} to i_L is at $2.7Rad$, however this can be chosen according to need. By changing ϕ, the generating or drive mode of each leg can be controlled. The DUT is operated at generating mode where diodes are more stressed whereas in control side IGBT's are more stressed. For optimal cooling conditions a Danfoss ShowerPower circulating a mixture of water and glycol is used [16]. The cooling temperature ($T_{cooling}$) is controlled by regulating heat dissipation through a heat exchanger using proportional-integral (PI) control.

C. Stressors and Converter Operating Parameter

In the present setup the primary operating parameters modulated to control test conditions are the current amplitude (i_L), fundamental frequency (F_{out}), and cooling temperature ($T_{cooling}$). The remaining converter working points are similar to real working parameters from a doubly fed induction generator (DFIG) rotor side wind power converter configuration, as given in Table I. The primary effect controlled through i_L and F_{out} is the change in junction temperature ΔT. However, when increasing ΔT one also affect the temperature gradient observed across the power module. $T_{cooling}$ is primarily controlled to increase the electrical and thermal resistance of the power module thereby increasing the effect of the current amplitude on switch loss.

TABLE I. CONVERTER OPERATING PARAMETERS

Symbol	Meaning	Offline	A-TC parameters
V_{DC}	DC link voltage	1000V	1000V
V_{DUT}	Forward voltage reference	$253V_{rms}$	$253V_{rms}$
i_L	Load current	$890A_{peak}$	$922A_{peak}$
θ	Phase (V_{DUT} to i_L)	$2.7Rad$	
F_{out}	Fundamental frequency		6Hz
F_{SW}	Switching frequency		2.5kHz
C	DC link capacitance	4mF	4mF
L	Inductor	380μH	380μH
$T_{cooling}$	Cooling temperature	80°C	80 ± 0.5°C

IGBT and diode chips are the primary contributors to the total power loss in the module. The total electrical power loss (P_{tot}) is

comprised of conduction (P_{cond}), switching (P_{sw}), and gate losses (P_{gate}), where the latter is normally neglected, see in Eq. (2).

$$\begin{aligned} P_{tot} &= P_{cond} + P_{sw} + P_{gate}, \\ &\approx P_{cond} + P_{sw}, \end{aligned} \tag{2}$$

In this example conduction losses include all forward losses during steady state which affects all current carrying components of the module (*Cu*, wires, chips, and solders). As illustrated in Eqs. (3) and (4), the power dissipation in the semiconductor chips during conduction depends on on-state period (t_{on}), on-state (υ_{ce}), and the load current (i_c) [17].

$$P_{cond,I} = \frac{1}{t_{out}} \int_0^{t_{on}} \upsilon_{ce}(t) i_c(t) dt, \tag{3}$$

$$P_{cond,D} = \frac{1}{t_{out}} \int_0^{t_{on}} \upsilon_{FD}(t) i_c(t) dt, \tag{4}$$

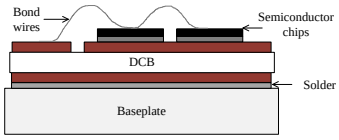
Switching losses include the energy required to turn-on and off the semiconductor components. For the diode this is limited to recovery loss, see (5). In Eq. (6) the IGBT switch-loss is presented [17].

$$P_{rec,D} = F_{sw} E_{rec} \left(\frac{V_{DC}}{V_{ref}} \right)^{K_{v,D}}, \tag{5}$$

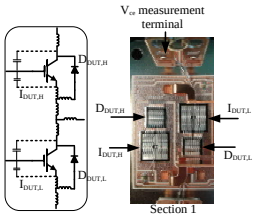
$$P_{sw,I} = F_{sw} E_{sw} \frac{i_c}{I_{ref}} \left(\frac{V_{DC}}{V_{ref}} \right)^{K_{v,I}}, \tag{6}$$

where I_{ref} and V_{ref} are the current and voltage at the manufacturer specified switching loss E_{sw} and recovery loss E_{rec}.

As illustrated in the power loss relation in Eqs. (2)-(6), the stress can be controlled through the load current, DC-link voltage, switching frequency, fundamental frequency and modulation index. The latter controls the stress between IGBT and diode. Fig. 5a shows a vertical



(a) Cross section of geometry.



(b) Layout of one section of open DUT.

Fig. 5. Vertical cross section of the IGBT module geometry and a layout of a section.

cross section of the geometry showing the layers constituting the IGBT module [1]. Similarly, a layout of a single section of open DUT is depicted in Fig. 5b.

III. Power Module

The tested power modules consist of six sections each rated at 1700*V* and total current of 1000*A*. Each section is comprised of two IGBT chips, two diodes, and 20 heavy *Al* bond wires placed on an ordinary direct copper bonded (DCB) substrate with an Al_2O_3 ceramic, as depicted in Fig. 5. All six sections are placed evenly on a *Cu* baseplate and the thickness of each layer is given in Table II.

TABLE II. THE THICKNESS AND COMPOSITION OF EACH LAYER.

Layer	Material	Thickness (μm)
Bond wire	*Al*	400
Metallization	*Al*	6
Chip	IGBT/Diode	200
Die attach	Solder paste	100
Copper	*Cu*	300
Ceramic	Al_2O_3	380
Copper	*Cu*	300
DCB attach	Solder paste	100
Baseplate	*Cu*	3000

IV. Wear out and Real Time Monitoring

The main parameter monitored during operation is the on-state υ_{ce}. Changes in the forward voltage originates from either electrical or thermal effects. The former could be due to degradation of interconnects (wire bonds, solder, metallization) or semiconductor chips, where the latter is primarily due to increase of thermal resistance. These are outlined in Fig. 6. Normally, both thermal and electrical effects affect the forward voltage at all times, but not necessarily at the same level. With continuous real time monitoring, the proposed method could indicate the origin which is responsible for the degradation.

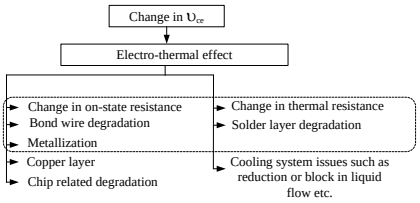


Fig. 6. υ_{ce} influencing degradations.

A. Measurement of On-state Voltage

An additional measurement circuit is added on top of the gate driver as shown in Fig. 7, which is able to measure on-state υ_{ce} in kelvin terminals of the module [18], [19]. As the υ_{ce} swings between *kV* and *mV* during transistor switching, the accuracy of the measurement circuit is essential. Two fast switching diode pairs (D_1/D_2 and D_3/D_4), as shown in Fig. 7, are used to block the off-state high voltage and measure the forward voltage drops on high/low side (HS/LS) of DUT. These BY203 diodes have a high breakdown voltage of 2*kV*, 300*nS* reverse recovery time, and zero forward voltage thermal coefficients at certain current level.

With HS IGBT on, D_1 and D_2 are forward biased with 10*mA*

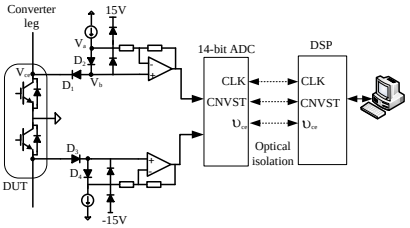


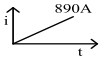
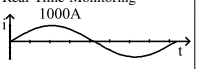
Fig. 7. An on-state υ_{ce} measurement circuit.

current source, they are thermally coupled externally and display similar forward voltage temperature coefficients [18]. The on-state υ_{ce} is measured using a bipolar 14-bit ADC with resolution of $0.61mV$. Eq. (7) is used to derive the absolute on-state υ_{ce}.

$$V_{ce} = 2V_b - V_a, \tag{7}$$

When the transistors are off, diodes (D_1/D_2 and D_3/D_4) blocks the high voltage to protect the resting part of the circuit. The on-state voltages are measured using two strategies, offline characterization and real time monitoring as given in Table III.

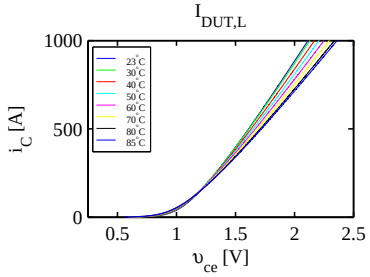
TABLE III. THE υ_{ce} MONITORING STRATEGIES.

υ_{ce} Monitoring Strategies	
Offline Characterization 	Real Time Monitoring 
The converter is in off state.	The converter is in operation.
The current ramp up from zero, through the device in micro seconds.	A PWM modulated sinusoidal current is used.
The υ_{ce} is measured at different current levels.	The chips have self heating due to power loss and increases υ_{ce}.
Limit the influence of temperature rise due to loading current.	Represent real on-state υ_{ce} drop.
The characterization is conducted at υ_{ce} load current.	Useful for wear out, temperature monitoring and lifetime investigation.
On-state forward resistance	Power module degradation

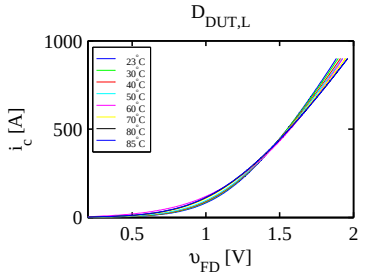
B. Offline Characterization

Offline characterization produces forward characteristics of all IGBT's and diodes in the power module. During characterization, the converter is stopped periodically every 5 minutes to measure the on-state υ_{ce} at load current from zero to $890A$. Throughout the test, the $T_{cooling}$ is maintained at $80^{\circ}C$. Before starting the process, the water temperature is maintained at $80^{\circ}C$ by circulating the liquid for a minute without electrically loading the device. The ramping process takes $340\mu S$ to characterize the DUT at one temperature level. The current-voltage (IV) characteristics for LS IGBT and diode for PM1 (Table V) are depicted in Fig. 8.

In offline characterization, power dissipation occurs mainly due to conduction losses which are limited by shortening the on-state period. The $I_{DUT,H}$/ $D_{DUT,L}$ and $I_{DUT,L}$/ $D_{DUT,H}$ pairs are conducting in DUT when current is positive and negative, respectively. The



(a) LS IGBT.



(b) LS diode.

Fig. 8. IV characteristics at different water temperatures for LS IGBT and diode.

measured υ_{ce} is a function of current, gate voltage (V_{GE}), and chip temperature. To study the change in υ_{ce} due to ageing, V_{GE} is kept constant at $15V$ and the $T_{cooling}$ is maintained steady at 80°C. The conduction time is in microseconds, hence υ_{ce} is a mainly function of applied current. At high current, the voltage drop is dominated by the on-state slope resistance which can be obtained from IV forward characteristics.

C. Real Time Monitoring

On-state υ_{ce}, υ_{FD} and corresponding i_C are measured at the middle of a PWM pulse. Hence, the sampling of online measurement is at $2.5kHz$. This method allows the settling time required by the circuit and packaging of the module to avoid transients in the measurement. In addition, this technique also makes implementation into the converter control simple. The measurement routine is illustrated in [19], where the online measurement is routined at every 5 min of operation to reduce the amount of data. During one measurement, the on-state υ_{ce}, i_C and corresponding $T_{cooling}$ are sampled and recorded for 2.5 cycles. The measurements for one cycle are demonstrated in Fig. 9.

1) Data Analysis: The measured voltages are analysed at $900A$ for both rising and falling sides of sinusoidal current. Any measurement point could in principle be chosen except at the crossover current where the behaviour of IGBT and diode changes from negative temperature coefficient (NTC) to positive temperature coefficient (PTC). Data interpolation is used in order to obtain the on-state υ_{ce} exactly at $900A$ on both sides. A window of $900 \pm 25A$ is used to improve the accuracy of the interpolation.

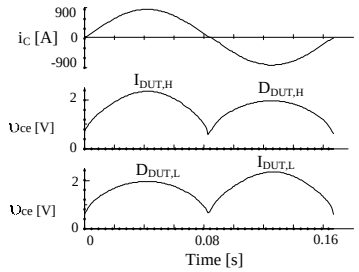


Fig. 9. Real time monitoring of on-state υ_{ce} and i_C for one cycle.

TABLE IV. THE ACTIVE COMPONENTS.

	Positive cycle		Negative cycle	
	P_{1+} (Rising)	P_{2+} (Falling)	P_{1-} (Rising)	P_{2-} (Falling)
IGBT	$I_{DUT,H}$ ($V_{ce,P1+}$)	$I_{DUT,H}$ ($V_{ce,P2+}$)	$I_{DUT,L}$ ($V_{ce,P1-}$)	$I_{DUT,L}$ ($V_{ce,P2-}$)
Diode	$D_{DUT,L}$ ($V_{FD,P1+}$)	$D_{DUT,L}$ ($V_{FD,P2+}$)	$D_{DUT,H}$ ($V_{FD,P1-}$)	$D_{DUT,H}$ ($V_{FD,P2-}$)

Table IV presents the analysing points and corresponding active components as shown in Fig. 10. By comparing the forward voltage

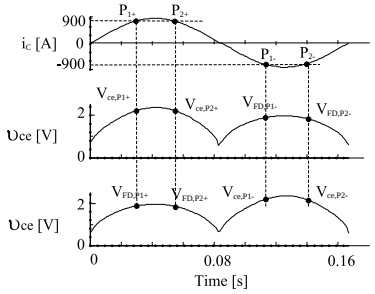


Fig. 10. Measurement study points.

$\upsilon_{ce}/\upsilon_{FD}$ at point P_{1+} and P_{2+} one obtaines an indication of themal responsivity of the active components, and similarly at P_{1-} and P_{2-}. The wear of tested module is demonstrated using on-state $\upsilon_{ce}/\upsilon_{FD}$ evolution at P_{1+}/ P_{1-}. For this analysis, a reference voltage $V_{P_{ref}}$ is obtained from the average of initial 100 healthy current cycles, as given in Eq. (8). The average voltage of first 100 cycles is $2.3531V$ with a standard deviation below $0.13mV$ for sample PM1. Eq. (9) measures wear of the DUT by displaying ΔV_1. The change in thermal responsivity is similarly measured by regarding the increase in forward voltage from P_{1+}/ P_{1-} to P_{2+}/ P_{2-}, namely ΔV_2 as given in Eq. (10). It is expected that the module will display slow steady wear in the beginning of the testing followed by accelerated wear closer to the end of life.

$$V_{P_{ref}} = \frac{1}{N}\sum_{i=1}^{100} V_{P_1}(n_i), \tag{8}$$

$$\Delta V_1(n) = V_{P_1}(n) - V_{P_{ref}}, \tag{9}$$

$$\Delta V_2(n) = V_{P_2}(n) - V_{P_1}(n), \tag{10}$$

where n index the number of cycles.

Considering half a fundamental cycle, the temperature cycle is expected to follow the current cycle because of the electrical power dissipation [20]. The temperature rise has a delayed response due to the thermal time constant. As a result, the on-state υ_{ce} is higher at P_{2+}/ P_{2-} at same current, regardless of material degradation.

D. Thermal Design

Regarding the geometry depicted in Fig. 5a-b, it is apparent that the direct line of thermal transport away from the *Si* chips is in the vertical direction through the DCB and baseplate. Accordingly, all four semiconductor elements from a module section have an identical primary thermal path. In Fig. 11 a simulated steady state thermal resistance from chip topside to backplate backside is presented. The resistance is derived by applying a fixed junction temperature and cooling flux to the given semiconductor component and baseplate, respectively. By varying the fixed values in a given range and solving the heat equation the resistance is obtained.

The linear shape of the thermal resistance is created by the

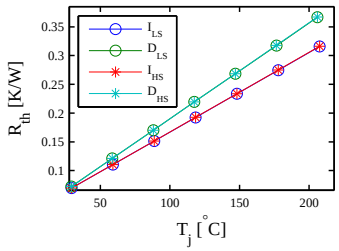


Fig. 11. Simulated steady state thermal resistance from chip to baseplate backside.

difference in volume between the chips and the remaining layers. A local heating of a chip, in the steady state, only provides limited module heating under the given cooling conditions, accordingly only the top layers affect the thermal resistance. However, thermal simulation provides a different result as discussed in [21]. In this paper a vast difference between the diode LS and HS due to the bond wire connections to the *Cu* pads is presented. This results in additional heating of the LS compared to the HS diodes and thereby additional stress.

V. Comparison of Test Specimens

Comparisons are carried out based on the on-state voltage variation of all four elements of the modules followed by a preliminary observation after removing the housing. PM1 is tested continuously until it fails, which is after 5.1×10^6 cycles of operation. This destructive test is regarded as a threshold to designate the number of test cycles for other modules under similar stress and loading. Test status is summarized for all modules in Table V.

TABLE V. Power module samples.

Power Module	Number of cycles	Status	Bond wire lift-off
0 (PM0)	0 cycle	Operational	No
1 (PM1)	5103000 cycle	Critical failure	All sections damaged
2 (PM2)	4500000 cycle	Operational	No
3 (PM3)	3526200 cycle	Operational	Section 1 diode HS wire 1 and 8 section 3 diode LS wire 6 to 10 Section 4 diode LS wires 8 to 10
4 (PM4)	2512800 cycle	Operational	No

A. Cooling Temperature Variation

Fig. 12 shows the mean water temperature $T_{cooling,m}$ on each fundamental cycle and the trend of variation during wear out test. The test is conducted in a closed room which ambient temperature varies periodically by up to 15°C during day and night. Table VI shows $T_{cooling,m}$ and their standard deviation (SD) during the test for four modules.

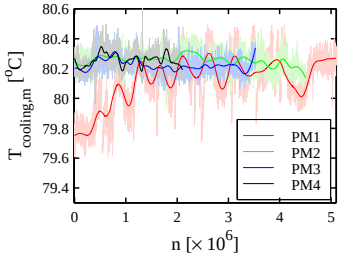


Fig. 12. Liquid cooling temperature variation for four tested modules.

TABLE VI. STATISTICS OF COOLING TEMPERATURE VARIATION.

Statistics	PM1	PM2	PM3	PM4
$T_{cooling,m}$ (°C)	80.12	80.25	80.23	80.26
SD (°C)	0.19	0.07	0.06	0.07

B. Results

Real time on-state υ_{ce} and υ_{FD} for both side IGBT's and freewheeling diode's are presented in Figs. 13-19. On-stage voltage evolution and ΔV_1 for $I_{DUT,H}$ are demonstrated in Figs. 13a-b, measured at $V_{ce,P1+}$. Similarly, on-stage voltage evolution and ΔV_1 for $I_{DUT,L}$ are demonstrated in Figs. 14a-b, measured at $V_{ce,P1-}$. The on-stage voltage evolution and ΔV_1 for $D_{DUT,H}$ are demonstrated in Figs. 15a-b, measured at $V_{FD,P1-}$. Similarly, the on-stage voltage evolution and ΔV_1 for $D_{DUT,L}$ are demonstrated in Figs. 16a-b, measured at $V_{FD,P1+}$. Figs. 17 demonstrates on-state voltage evolution at P_{1+} and P_{2+} on $I_{DUT,H}$.

Figs. 18a-b demonstrates the ΔV_2 for $I_{DUT,H}$ and $D_{DUT,H}$ respectively as described in Eq. (10). Similarly, Figs. 19a-b demonstrates the ΔV_2 for $I_{DUT,L}$ and $D_{DUT,L}$.

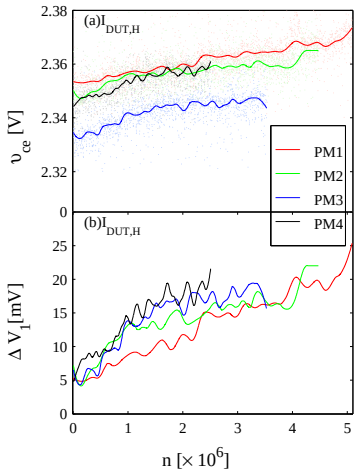


Fig. 13. (a) On-state υ_{ce} on $I_{DUT,H}$, (b) ΔV_1 at $I_{DUT,H}$ at 900A.

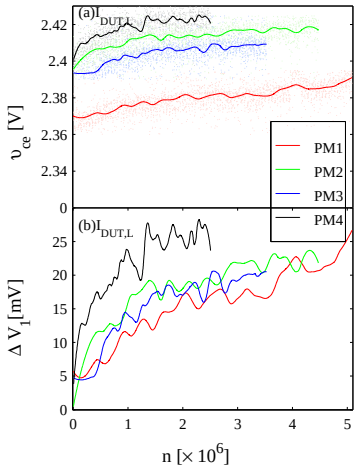


Fig. 14. (a) On-state υ_{ce} on $I_{DUT,L}$, (b) ΔV_1 at $I_{DUT,L}$ at 900A.

C. Post-Test Analysis

Preliminary investigations of the tested power modules after removing the housing are presented in Table V. The LS diode is damaged severely in normal wear out in comparison to other elements of the module. Although PM3 is functional, the LS diode in one section is severely damaged. Fig. 20 shows image of PM1, where the majority of the semiconductor chips are failed.

1) Chip Metallization: In Fig. 21 four SEM images of the metallization surface is presented for the IGBT and diode from a new

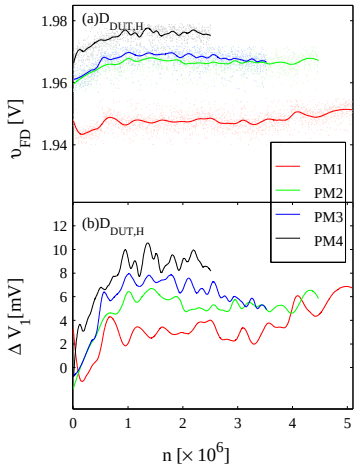


Fig. 15. (a) On-state υ_{FD} on $D_{DUT,H}$, (b) ΔV_1 at $D_{DUT,H}$ at 900A.

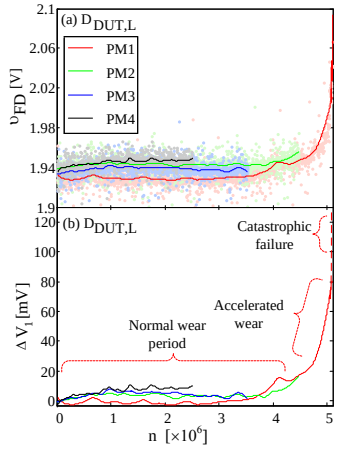


Fig. 16. (a) On-state υ_{FD} on $D_{DUT,L}$, (b) ΔV_1 at $D_{DUT,L}$ at 900A.

module (PM0) and from the PM3 LS IGBT and diode. In PM0 and PM3 LS IGBT, no visible changes are observed in the metallization. In contrast the diode LS in PM3 shows considerable reconstruction. This mechanism was only observed in the diode metallizations.

2) Micro-Sectioning: In Fig. 22 cross-sectional images of a wire bond from sample PM1 is presented. The cross-sectional image is obtained using micro-sectioning followed by electro-etching and optical microscopy with polarized light, see [15] for details concerning the approach.

In Fig. 22 the *Al* grain structure is clearly observed. The grains range from 30 to 100μm in diameter from the bonded region and

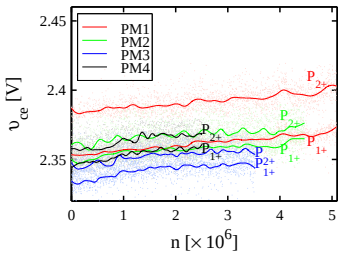


Fig. 17. On-state υ_{ce} comparing at $I_{DUT,H}(V_{ce,P1+})$ and $(V_{ce,P2+})$ at 900A.

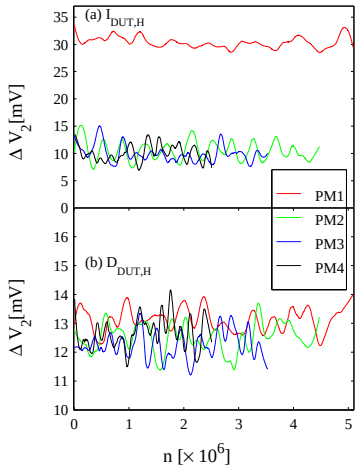


Fig. 18. (a) ΔV_2 at $I_{DUT,H}$ and, (b) ΔV_2 at $D_{DUT,H}$ at 900A.

inwards the *Al* wire. A partial wire delamination is observed between the wire and the metallization with only limited cracking inside the wire itself. In the examined samples there was a general tendency that fractures occured closer to the chip surface than normally. Furthermore, cracks were on several occasions observed to move inside grains instead of along boundaries. This indicates poorly bonded wires and that the bond itself were the weakest element.

VI. Discussion

The drop in forward voltage depends upon parameters such as on-state resistance which includes *Cu* terminals, *Al* bond wires, *Cu* layer, chip resistance, load current and device cooling temperature. Figs. 13-17 shows variation in conduction voltage drop for four different modules at the same working conditions as presented in Table I. The difference in off-set of the forward voltage observed between PM1-4 is due to differences in module production. Starting on-state υ_{ce} varies with nearly 20mV to 30mV in both HS and LS IGBTs, however, this is clear from ΔV_1 in Figs. 13b and 14b the voltage drop rise follows the same trend with number of cycles. Similarly, HS and

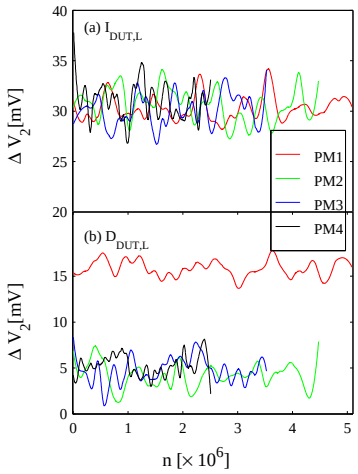


Fig. 19. (a) ΔV_2 at $I_{DUT,L}$ and, (b) ΔV_2 at $D_{DUT,L}$ at 900A.

Fig. 20. PM1 module after removal of housing, busbar, and silicone gel. The majority of semiconductor chips are failed.

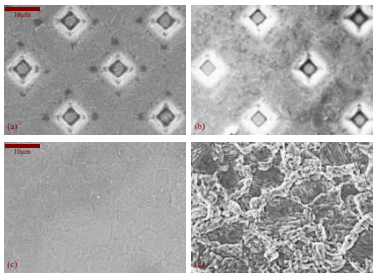


Fig. 21. SEM images of the metallization surface of: (a) PM0 IGBT, (b) PM3 LS IGBT, (c) PM0 diode, and (d) PM3 LS diode.

LS diodes have 20mV variation between the four modules. Fig. 16b showing the change in ΔV_1 for $D_{DUT,L}$ also shows that the increased off-set does not indicate potential early failures.

In Fig.16 υ_{FD} increases significantly between 4×10^6 and 5×10^6 giving an indication of large change in resistance of PM1. The voltage drop was increased by 135mV just before explosion, which is nearly 7% rise in initial voltage drop. The on-state υ_{ce} on LS also increased by nearly 20mV, this is close to 1% rise indicating the IGBT did not fail initially. Step increments in υ_{FD} are observed after crossing the

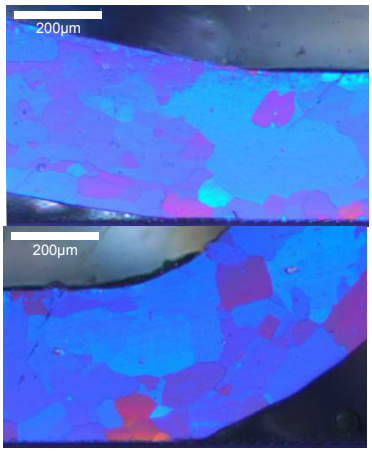


Fig. 22. Cross-sectional images of wire bond in sample PM1 obtained using micro-sectioning combined with electro-etching.

4.5×10^6 cycles of operation, indicating possible bond wire lift-off during the operation. Nearly 7-10mV step increment are witnessed for LS diode of PM1. This is consistent with the micro-sectioning results presented in Sec. V-C2. Here the bonded interfaces were identified as clear weak spots in the module geometry, and several lifted/delaminated wires were observed.

Figs.18 and 19 shows thermal responsivity of the HS and LS diodes of the DUT. The sample with a mean value above the rest appear to be the same sample displaying higher variation in baseplate temperature in the cooling (12). This could indicate a difference in cooling conditions. The oscillation amplitude appear on the scale of 5-8mV, this is expected to be due to standard noise during the measurement. Lack of changes in the thermal responsivity shows that the solder is not degrading on a scale which changes the signal above the *SD*. The reason for this is also proven in [22] where four point probing is applied to single out degrading elements.

In Figs. 21a-d topographic images of the surface metallization are presented. A clear difference between the IGBT and diode metallization is observed. While the IGBT metallization seems unaffected after 3.5×10^6 cycles the diode metallization is severely reconstructed. This is in accordance with the expected power loss explained in Sec. II.

VII. Conclusion

The two primary outcomes of this paper are; (1) an online monitoring system able to handle realistic field stress conditions of power modules and (2) data evaluation theory separating wire and solder degradation. From online monitoring, nearly 20mV variation in on-state voltage drop is measured between the modules for all IGBT's and diodes because of unmatched geometrical structure in production. A method re-calibrating automatically on each individual device is presented removing effects from difference in geometry from the results. Solder degradation is realized by measuring thermal responsivity which also varies in accordance with the cooling between the modules. No major failure in solder or thermal system is found, which is also supported by [22]. Primary degradation is observed by

changes in relative forward voltage ΔV_1 indicating wear of bond wire interconnects and chip metallization. This is consistent with post test analysis based on micro-sectioning, SEM, and four-point probing of electrical parameters. The latter is presented in [22]. To summarize, the presented online monitoring technique is possible to implement in real life application and display possibilities of separating degradation patterns of different interconnects.

REFERENCES

[1] J. Lutz, H. Schlangenotto, U. Scheuermann, and R. D. Doncker, *Semiconductor power devices*. Springer, 2011.

[2] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 708–719, 2012.

[3] P. Cova and F. Fantini, "On the effect of power cycling stress on igbt modules," *Microelectronics Reliability*, vol. 38, no. 6-8, pp. 1347–1352, June-August 1991.

[4] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of igbt modules in traction application," *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, vol. 1, pp. 425–430, May 1997.

[5] A. Morozumi, K. Yamada, T. Miyasaka, and Y. Seki, "Reliability of power cycling for igbt power semiconductor modules," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, vol. 3, Sept 2001, pp. 1912–1918.

[6] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, pp. 653 – 667, 2002.

[7] U. Scheuermann, "Reliability challenges of automotive power electronics," *Microelectronics Reliability*, vol. 49, pp. 1319 –1325, 2009.

[8] H. Berg and E. Wolfgang, "Advanced {IGBT} modules for railway traction applications: Reliability testing," *Microelectronics Reliability*, vol. 38, no. 68, pp. 1319 – 1323, 1998.

[9] "Power cycling," *JEDEC Standard*, no. JESD22-A122, August 2007.

[10] "Power and temperature cycling," *JEDEC*, no. JESD22-A105C, January 2011.

[11] V. Smet, F. Forest, J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of vce monitoring as a real-time method to estimate aging of bond wire-igbt modules stressed by power cycling," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 7, pp. 2760–2770, July 2013.

[12] H. Huang and P. Mawby, "A lifetime estimation technique for voltage source inverters," *Power Electronics, IEEE Transactions on*, vol. 28, no. 8, pp. 4113–4119, Aug 2013.

[13] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (igbt) prognostics," *Reliability, IEEE Transactions on*, vol. 58, no. 2, pp. 271–276, June 2009.

[14] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in igbt modules for electric vehicle drives," *Power Electronics, IEEE Transactions on*, vol. 28, no. 12, pp. 5568–5577, Dec 2013.

[15] K. B. Pedersen, P. K. Kristensen, V. Popok, and K. Pedersen, "Micro-sectioning approach for quality and reliability assessment of wire bonding interfaces in {IGBT} modules," *Microelectronics Reliability*, vol. 53, no. 9-11, pp. 1422 – 1426, 2013.

[16] K. Olesen, R. Bredtmann, and R. Eisele, ""shower power" new cooling concept for automotive applications," in *Automotive Power Electronics*, June 2006.

[17] A. Volke and M. Hormkamp, *IGBT Modules Technologies, Driver and Applications*, 2nd ed. Infineon Technologies AG, 2012.

[18] S. Beczkowski, P. Ghimire, A. de Vega, S. Munk-Nielsen, B. Rannestad, and P. Thøgersen, "Online vce measurement method for wear-out monitoring of high power igbt modules," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sept 2013, pp. 1–7.

[19] P. Ghimire, A. de Vega, S. Beczkowski, S. S.Munk-Nielsen, B. Rannestad, and P. B. Thøgersen, "Improving power converter reliability: Online monitoring of high-power igbt modules," *Industrial Electronics Magazine, IEEE*, vol. 8, no. 3, pp. 40–50, Sept 2014.

[20] P. Ghimire, K. B. Pedersen, A. R. d. Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thøgersen, "A real time measurement of junction temperature variation in high power igbt modules for wind power converter application," in *Integrated Power Systems (CIPS), 2014 8th International Conference on*, Feb 2014, pp. 1–6.

[21] K. Pedersen and K. Pedersen, "Dynamical electro-thermo-mechanical simulation of material degradation in high power igbt modules," *Microelectronics Reliability*, 2014, submitted to IEEE Transaction on Power Electronics.

[22] K. B. Pedersen, L. H. Ostergaard, P. Ghimire, V. Popok, and K. Pedersen, "Degradation mapping in high power igbt modules using four-point probing," 2014, submitted to Transactions on Device and Material Reliability.

PAPER F

Dynamic modelling method of electro-thermo-mechanical degradation in IGBT modules

Dynamic Modelling Method of Electro-Thermo-Mechanical Degradation in IGBT Modules

Kristian Bonderup Pedersen and Kjeld Pedersen

***Abstract*—A degradation model investigating the electro-thermo-mechanical fatigue, experienced by insulated gate bipolar transistors modules, is presented. To illustrate the concept a specific case of power modules subjected to active power cycling which induce failure through bond wire lift-off is considered. Bond wire lift-off is believed to be due to thermally induced stress arising from a mismatch in the coefficients of thermal expansion between the wires and the given substrate. Overall, the theoretical evaluation is based on determining the thermo-mechanical stress around the bond wire/substrate interface through multiphysics based models. The simulation detail and included equations are specified according to region of interest and their complexity. In common, however, is the use of the finite element method combined with empirical equations. The final result is a numerical approach to evaluate the damage accumulated by a given load which may be used for prediction of lifetime or optimization of work points and module geometry.**

I. Introduction

DEMANDS of increased use of renewable energy sources as well as changes in the structure of the power grid towards a more distributed system makes the global electrical energy consumption increase steadily. Accordingly, reliable and efficient power electronics is essential[1]. In wind power systems failures in the power converters account for as much as 15% of all failures. Degradation assessment of individual elements as well as accurate lifetime estimation of power modules is thus vital. Presently, insulated gate bipolar transistor (IGBT) modules are used widely, with applications ranging from a few $100W$ to several MW. Accordingly, a modelling method needs to be developed which is usable in a wide application range. This requires a detailed model of the physics-of-failure of the device of interest.[2], [3]

In the present paper the problem of power modules employed in high power conversion is regarded. Thermo-mechanical fatigue accounts for several severe failure modes of IGBT modules, e.g. solder creep, bond wire lift-off/heel cracking, metallization reconstruction, etc. [2], [4]. This is normally induced by time varying loads (alternating currents, pulsed conditions, etc) which causes local heating in active components followed by cooldown during passive periods. In the present paper a model for degradation analysis of high power IGBT modules is presented. In this case a power module subjected to active power cycling is regarded, were the dominant failure mechanism observed is bond wire lift-off[5], [6].

Given the highly varying loads experienced by this type of component it is not surprising that thermo-mechanics play an important role on its lifetime. If the primary load of the overall module is the applied current and the switching of it, then the dominating heating occurs in the active components - transistors and diodes. Due to the vast difference in the volume of the chips and the remaining part of the module one distinguishes between two types of loads, namely long and short load times. In both cases the diodes and transistors are heated up followed by the surrounding layers. But in the latter case the short time between heat-up and cool-down of regions ensures that only active elements and immediate contacts are significantly heated[3], [7].

So far the common approach in degradation and lifetime assessment of IGBT modules failing due to bond wire lift-off has been based on the Coffin-Manson (CM) or CM-Arrhenius (CM-A) model with a parameter corresponding to the load inserted [8], [9], see Eqs. (1)-(2). Often the change in temperature ΔT is used as the load and the model parameters are fitted to accelerated test data to take shape, environment, degree of damage, etc. into account, see [3], [5], [6], [10], [11].

$$N_f = \beta \left(\Delta T\right)^{\alpha}, \tag{1}$$

$$N_f = \beta \left(\Delta T\right)^{\alpha} \exp\left\{\frac{E_A}{k_B T}\right\}, \tag{2}$$

where N_f is number of cycles to failure, α and β are fitting parameters, and E_A is an activation energy.

The simplicity of the models is both the advantage and disadvantage. In principle they can be applied to any element failing from thermo-mechanical induced degradation, however, one needs to obtain component specific parameters from fitting to test data. In high power electronics the expected component lifetime often exceeds 10 years, accordingly, one needs accelerated conditions to obtain lifetime information within a reasonable time frame. This is also the normal approach, were the component of interest is subjected to highly accelerated test conditions, e.g. a high ΔT, that normally cause a failure in a shorter time frame (days-weeks). α and β are afterwards obtained by fitting the model to accelerated test data, and the lifetime at non-accelerated conditions are obtained through extrapolation. While this approach has been useful for more than a decade, it has

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begun to be problematic in recent years. There are several reasons for this:

1) The simplicity of the model does not take the effect of geometry and material composition into account. It has been reported that changes of e.g. wire curvature alone as well as bond footprint affect the lifetime directly[12], [13]. Accordingly, accurate fitting of empirical models is paramount.
2) With ΔT as only input parameter and only one set of fitting parameters attached to the stressor, the model assumes the eventual failure is either a single mechanism or a series of mechanisms connected to ΔT with a constant grouping.
3) Failure mechanisms observed under accelerated conditions are not necessarily occurring at normal operation.
4) Variation in production quality requires a very large quantity of wear-out tests.[10]
5) ΔT is often based on thermal networks or the V_{CE} which corresponds to the average chip temperature. Due to the geometrical shape and the change of the load over time and space it is fair to assume that the temperature field is not constant everywhere. On the contrary it has been noted that depending on the load, a very inhomogeneous field might be the case[12], [14].

The first problem has in later years been sought solved by increasing the number of fitting and input parameters in the same way the Arrhenius factor was added in Eq. (2), see [9], [15], [10]. However, this still only delivers a functioning lifetime model at accelerated conditions as well as for the particular module tested.

In the following a dynamic 3D degradation model which can be used for design optimization, specification of load limitations, and lifetime estimation is presented.

II. Model Structure

In principle all degradation models in cyclic systems are based on the same steps: *load, damage, recovery*. These process steps run simultaneously and do so until reaching a given failure condition. To construct a degradation model for electro-thermo-mechanical degradation of interconnects in high power IGBT modules, one need to understand the load conditions, relevant sub-components, and degrading elements. The power modules of interest are primarily used for power conversion in high power application fields, e.g. wind mills or automotive. Based on this the model presented in Fig. 1 is proposed.

Due to the complexity of the regarded system, the model is as far as possible sought divided into steps. In Figure 1 four primary sections constitute the model: *(1) power loss, (2) temperature field, (3) solid mechanics*, and *(4) material degradation*. These are all directly connected as illustrated by the lines in the flow chart.

III. Geometry and Test Conditions

The proposed model can be utilized on any geometry, however, in order to validate the simulation results an actual IGBT module is regarded which in [16] and [17] is subjected to accelerated testing.

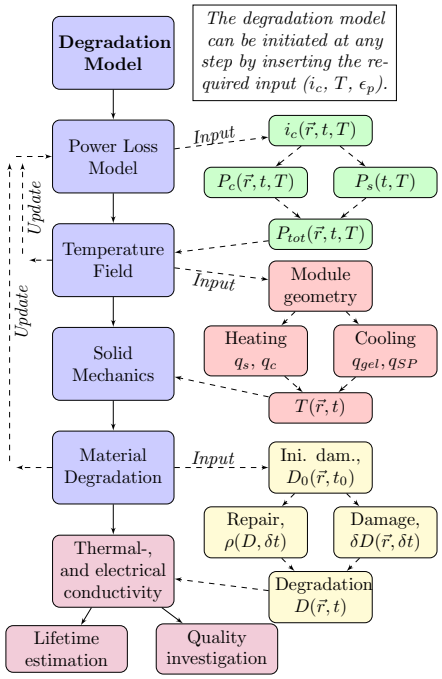


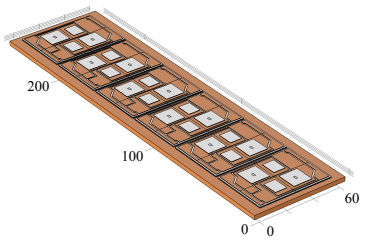
Fig. 1. Flow chart of electro-thermo-mechanical degradation model of power module interconnects.

A. Power Module Geometry

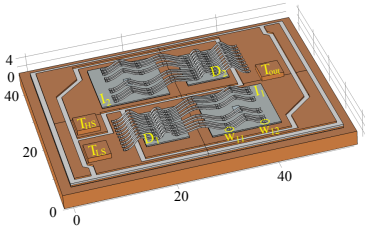
The considered module consists of six identical sections with two IGBT chips and two diodes. Each section is rated at $1700V$ and a total current of $1000A$ of all six. The geometry is depicted in Figs. 2a and 2b with the layer thickness specified in Table I.

B. Sinusoidal Test Conditions

The specific test conditions are presented in Table II and a detailed description of the setup is outlined in [17]. A sinusoidal current load is applied at $6Hz$ and switched at $2.5kHz$. Water cooling is applied directly to the backside of the baseplate using Danfoss ShowerPower, see [18]. The high load current combined with a high cooling temperature and low fundamental frequency is a common approach for causing accelerated wear in this type of power module.



(a) Full power module with limited elements included.



(b) Detailed illustration of single module section.

Fig. 2. CAD illustration of a full power module (a) and a single section (b). The power module consist of six identical sections running in parallel.

TABLE I
LAYER COMPOSITION AND THICKNESS OF THE DCB BASED IGBT MODULE.

Layer	Material	$\mathbf{d_i}$ [μm]
Bond wire	Al	400
Metallization	Al	6
Chip	IGBT/Diode	200
Solder	$SnAg(3.5)$	100
Copper	Cu	300
Ceramic	Al_2O_3	380
Copper	Cu	300
Solder	$SnAg(3.5)$	100
Baseplate	Cu	3000

IV. THEORY

This chapter contains the fundamental theory behind the degradation model. As discussed in Section II the model is separated into a number of blocks, the theory is outlined similarly.

A. Power Loss

In Section III-A a typical power module design is presented. This consist of several active and passive components. While power losses in passive components (Cu pads, Al bond-wires, solders, metallizations) can be limited to standard conduction losses the active semiconductor components have several other contributing effects. The power loss in the semiconductor components far exceed the conduction losses of the remaining elements, accordingly the power loss calculation is centered around the semiconductor chips.

TABLE II
ACCELERATED TEST CONDITIONS.

Parameter	Symbol	Value
DC-link voltage	V_{DC}	$1000V$
Peak load current	I_{tot}	$922A$
Fundamental frequency	f_{out}	$6Hz$
Switching frequency	f_s	$2.5kHz$
ShowerPower temperature	T_{SP}	$80°C$

The total power loss in a power module is normally separated into static (P_{static}), switching (P_s), and driving losses ($P_{driving}$):

$$P_{tot} = P_{static} + P_s + P_{driving} \tag{3}$$
$$\approx P_c + P_s \tag{4}$$

In Eq. (4) P_{static} includes conduction losses (P_c) and blocking losses. As the forward blocking and driving losses are often small compared to the remaining these are normally left out. [19], [20], [21]

In the test system regarded, a well-defined current load is applied, see [16], [17]. Accordingly, conduction losses in all passive components are calculated by deriving the current distribution ($i_c(\vec{r},t)$) and using the local electrical conductivity. However, for the active components switching losses has to be included as well. As explained in [16], the load is switched between IGBTs and diodes and similarly it changes between interconnects. This is handled through the system modulation function (m):

$$P_c^{IGBT} = i_c(\vec{r},t)v_{CE}(\vec{r},t,T)\left(\frac{1-m}{2}\right), \tag{5}$$

$$P_s^{IGBT} = f_s\left[E_{on}(T)+E_{off}(T)\right]\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v^I}, \tag{6}$$

$$P_c^{Diode} = i_F(\vec{r},t)v_D(\vec{r},t,T)\left(\frac{1+m}{2}\right), \tag{7}$$

$$P_{rec}^{Diode} = f_s\left[E_{rec}(T)\right]\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v^D}, \tag{8}$$

where i and v denote the forward current and voltage of the semiconductor components and K_v is the shape difference[21] of the switch-loss curve (E) at V_{DC} compared to V_{ref} in the data-sheet.

As introduced through the arguments of the power losses in Eqs. (5)-(8) the switching and recovery loss is assumed homogeneously distributed according to temperature.

B. Electro-Thermal Model

The electro-thermal modelling may be divided into the actual power loss presented in Sec. IV-A which heats up the component and the following transfer of heat. Accordingly, the physical parameters of the geometry as well as the geometrical structure is important for the temperature field.[14]

1) Transient Temperature Fields: As earlier discussed the initial problem is to calculate the temperature field for a given load. This problem is fundamentally governed by the diffusion-convection-reaction partial differential equation (PDE), which is, when neglecting mass transport, given as [22], [23]

$$\vec{\nabla} \cdot (k\vec{\nabla}T(\vec{r},t)) + \frac{\partial q(\vec{r},t)}{\partial t} = \rho c_p \frac{\partial T(\vec{r},t)}{\partial t}. \quad (9)$$

Here ρ is the density, c_p is the specific heat capacity, k is the thermal conductivity, and q is the heat flux. In the stationary case this problem is ideal for an finite element (FE) approach. However, as the load fluctuates with the applied current the problem is far from stationary. It may still be solved using an FE analysis, but with significantly higher demands on computational power and solution time. As mentioned in the previous section the power loss fluctuates in time and space when the load switches to either one of the diodes or the other transistor.

2) Physical Parameters: In order to accurately calculate $T(\vec{r},t)$ for the power module presented in Sec. III-A temperature dependent parameters are needed[14], [24]. For pure materials like Al and Cu this is catalogued data if one assumes the materials as continua, see [24] or [25]. However, for the semiconductor devices the situation is different which is clearly seen in Fig. 3:

Fig. 3 presents a topographic view and a FIB cut of a new

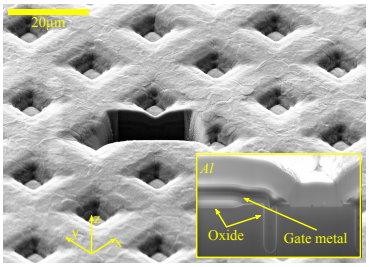
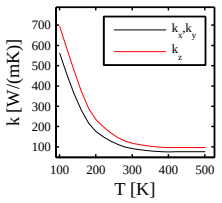


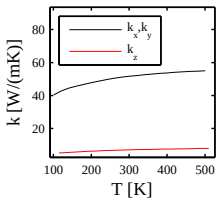
Fig. 3. SEM image of the topological layout of an IGBT chip with a FIB obtained cross-sectional view of the trench gate structure.

IGBT chip. In the topographic image a channel like structure of the IGBT is observed with a spacing of app. $18\mu m$. In the FIB cut the vertical layout near the chip surface is observed. From the top down the first $6\mu m$ is Al metallization. Beneath the metallization two regions are observed: the current channel and the gate area. The current channel consists of doped Si (see the dark grey region of the bottom of the FIB cut in Fig. 3) and the gate area includes the gate metal region surrounded by a thin white oxide layer.

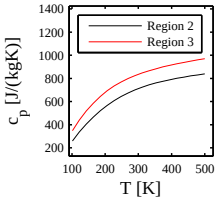
The gate structure seen in the IGBT chip in Fig. 3 is far from a continuous medium and accordingly a different approach needs to be applied with regard to physical parameters. Presently, an effective medium approach (EMA) is applied for the calculation of the thermal conductivity tensor and the specific heat capacity. A similar approach is applied in [14] for a trench based structure. Here a channel type



(a) Thermal conductivity of region 2. The components in the direction parallel to the chip surface are identical due to symmetry.



(b) Thermal conductivity of region 3.



(c) Pressure specific heat capacity of regions 2 and 3.

Fig. 4. Thermal conductivity and specific heat capacity of regions 2 and 3 as a function of direction and temperature. The parameters are derived using an EMA.

transistor is considered as seen in Fig. 3. Most of the materials in the composition are well known with regard to thermal conductivity and specific heat capacity. For the doped silicon the temperature dependent parameters are obtained from [26].

The IGBT geometry is separated into three regions, the first region includes all layers from the solder to the beginning of the trench in Fig. 3. This is the major part of the chip, and due to its simple structure its physical parameters may be derived directly from the doping. Region 2 extends from the bottom of the trench to the beginning of the horizontal oxide layer, resulting in identical coefficients in two directions. This leaves the remaining layers in region 3 including the horizontal oxide and gate layer. The simulated thermal conductivity and specific heat capacity of regions 2 and 3 are presented in Figs. 4a-4c:

Due to symmetry considerations the thermal conductivity in the plane of the chip surface are identical. The clear difference between region 2 and 3 is generated by the volume fraction of the oxide layer which has a much lower thermal conductivity. With the amount of silicon present, the heat capacity naturally comes close to that of bulk silicon.

3) Boundary Conditions: The bottom of the baseplate is in this example directly water cooled and the topside is cooled through the gel. Both of these imply a convection surface, the water cooling externally forced and the gel passively. The convection surface on the gel side is not to be confused with the assumption that mass transport are occurring inside the silicone gel. It is merely an approach to model the flux through the gel without including its vast volume into the model. The

convection surfaces are approached using a BC with Newton's law of cooling:

$$q_n = -h_s(T - T_\infty), \tag{10}$$

where q_n is the flux normal to the surface, h_s is the mean coefficient of convection of the surface, and T_∞ is the stationary temperature of the ambient beyond the thermal layer. The convection parameter for the Danfoss ShowerPower system is obtained from [18] and the gel is modelled as passive cooling in air.

C. Thermo-Mechanical Modelling

In the same way the calculation of the temperature field depends heavily on the electro-thermal parameters, the derivation of the plastic strain field depends highly on the CTE, elastic parameters, and yield strength. However, the primary damage assessment is carried out in the degradation calculation based on sample specific experimental data. Accordingly, textbook parameters are used in the stress derivation and corrected afterwards.

With the simulated temperature field $T(\vec{r}, t)$ the thermal expansion may be derived directly. The created strain is uniform leaving out shear contributions:

$$\vec{\epsilon}_{th} = \Delta\vec{\alpha} \cdot \Delta T, \tag{11}$$

where $\vec{\alpha}$ is the CTE vector which reduces to α for linear isotropic materials [22, Ch.7]. For two continuous slabs connected to each other the three strain components $\epsilon_x, \epsilon_y, \epsilon_z$ are easily calculated through the difference in CTE and the fundamental constraints between the three directions. From these components the generated plastic strain for a single cycle may be derived analytically from a 1D approximation presented in [27]. This approach, however, neither take the geometry or an inhomogeneous temperature field into account. The difference will be clear in the results section where results from the detailed $3D$ dynamical simulation is presented together with the simplified.

By combining Eq. (11) with the before mentioned temperature field the resulting displacement field $u(\vec{r}, t)$ may be calculated everywhere. To identify when the strain moves from the elastic to the plastic regime the stress needs to be derived. In the elastic region this is solved through the elasticity tensor. In the inelastic regime the solution is more problematic. In the present case the plastic potential function $(F(\vec{\sigma}))$ is used to calculate changes in the plastic deformation:

$$\frac{d\epsilon_p}{dt} = \frac{d\lambda}{dt}\frac{\partial F(\vec{\sigma})}{\partial \sigma}, \tag{12}$$

where λ is the plastic multiplier and $F(\vec{\sigma})$ for a Von Mises type isotropic strain-hardening material is

$$F(\vec{\sigma}) = \sigma_{VM}(\vec{r}) - \sigma_y(\vec{r}), \tag{13}$$

where σ_{VM} is the Von Mises stress, and σ_y is the yield strength of the material. To account for material hardening over time $\sigma_y(\vec{r})$ needs to be modified continuously. However, in the present model the material hardening is included in the degradation step, meaning that material hardening is in the structural mechanics calculation assumed perfectly plastic.[28]

D. Degradation Modelling

The thermal and mechanical analysis presented in Sec. IV-B and IV-C in principal yields all the primary stressors relevant for modelling degradation in power module interconnects. However, the derivation of the actual material degradation as a function of position and time $(D(\vec{r}, t))$ induced by the stressors is non-trivial. The primary failure mechanism experienced in the presently regarded module placed under the conditions shown in Table II has been identified as bond wire lift-off and metallization reconstruction, see [29]. In [8], [30] a 1D approach for modelling the bond wire lift-off failure mechanisms is presented. The model is a time-domain based degradation approach where T and ϵ_p are inputs and the fracture propagation criteria is obtained from shear tests:

$$\begin{aligned}\delta D &= f(D, \epsilon, T)\delta T - \rho(D, T)\delta t \\ &= f_\epsilon f_D f_T \delta T - \rho_D \rho_T \delta t\end{aligned} \tag{14}$$

In Eq. (14) the first term on the right hand side includes the created damage during loading and the second term the damage removal. In the following two sections the terms applied in Eq. (14) in this paper is presented for damaging and repairing effects, respectively. The main function $D(\vec{r}, t)$ of the differential equation in Eq. (14) is a unitless degradation parameter. Any physical interpretation of the absolute value of $D(\vec{r}, t)$ has to be obtained by comparing to specified criteria, e.g. fracture propagation by comparison to experimental data or design quality by comparison to damage generated at other positions.

1) Damage functions: The first term on the right hand side of Eq. (14) is the damage generated at time t. As indicated in the equation this is separated into four contributions: Strain concentration function $f_\epsilon(\vec{r}, t)$, hardening function $f_D(\vec{r}, t)$, thermal load $f_T(\vec{r}, t)$, and a local displacement strain $d\epsilon_d$:

$$f_\epsilon(\vec{r}, t) = G_0 {\epsilon_p}^e(\vec{r}, t), \tag{15}$$

$$f_D(\vec{r}, t) = 1 + a_H D(\vec{r}, t)^{B_H}, \tag{16}$$

$$f_T(\vec{r}, t) = \left(\frac{T_{eq}}{T(\vec{r}, t)}\right)^{B_T}, \tag{17}$$

$$d\epsilon_d = \Delta\alpha\delta T, \tag{18}$$

where G_0, a_H, B_H, and B_T are computational coefficients and ${\epsilon_p}^e$ is the effective plastic strain.

2) Restoration functions: The second term on the right hand side of Eq. (14) is the recovery part. ρ_D is the already existing damage and $\rho_T \delta t$ is a temperature activated annealing term depending on the amount of time at the given temperature and the strain hardening experienced prior,

$$\rho_T(\vec{r},t) = \kappa_2 \exp\left(-\frac{E_A}{k_B T(\vec{r},t)}\right), \tag{19}$$

where E_A is the activation energy and κ_2 is a computational coefficient.

V. Results

As is clear from Secs. III and IV the regarded geometry and theory combined compose a complicated problem which was the motivation for separating the modelling into multiple blocks as illustrated in Fig. 1. Apart from separating the simulation into multiple steps, the detail level of the applied theory also depends the on regarded geometry. An example of this is that thermal simulations are initially carried out on a full module as presented in Fig. 2a to obtain information on thermal interactions between sections. In this simulation the wire bonds are not included as the local effect, they are observed to have on the chip surface temperature, only has limited influence on the thermal overlap of the sections. Accordingly, in the initial step of the temperature field calculation a function of the baseplate surface temperature ($T_{BP}(\vec{r},t)$) is obtained and used as input in the detailed simulation of the chip temperature. Similarly, the detail level of the strain field and degradation function calculation is also increased when regarding a more specific region.

The results section is separated into individual model steps and module/section/bond wire analysis.

A. Temperature Field

With the sinusoidal applied load the temperature field of the geometry presented in Figs. 2 varies highly in time and space. If the simulation is initiated at the same temperature as the cooling water (T_{SP}) the applied power loss initially increases the mean temperature of the four active components until reaching a steady level. With a sinusoidal load more than 30 power cycles are needed to reach a steady level.

1) Module Temperature Field: In Fig. 5 the mean temperature of the topside and backside of the baseplate is plotted along a line placed at the center running parallel to the module long side. The curve is plotted at four time steps during a power cycle, where $t = 0$ notes the beginning of a steady cycle.

The flow rate in the Danfoss ShowerPower is specified so the temperature of the cooling water varies less than $0.5°C$. Accordingly, the baseplate backside temperature is seen to be close to T_{SP} even near the middle of the plate where the majority of heat dissipates. Similarly, the baseplate topside is close to the backside temperature with limited effect of the chosen time during a power cycle. Finally, with a homogeneous convection approximation on the baseplate backside, as introduced in Sec. IV-B, the section position is seen to have limited effect on the baseplate surface temperature. An effect is observed when regarding the situation in 3D. Here, due to the homogeneous boundary condition, the distribution is mirrored around the center of the module and small edge effects are observed on sections 1 and 6.

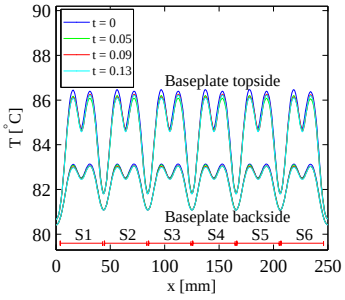


Fig. 5. Baseplate mean temperature of topside and backside plotted along a line placed at the module center. The position and width of the different sections are marked with red lines.

2) Junction Mean Temperature: With the parameters presented in Tab. II the mean junction temperature of the four chips are as presented in Fig. 6. In Figs. 7 the

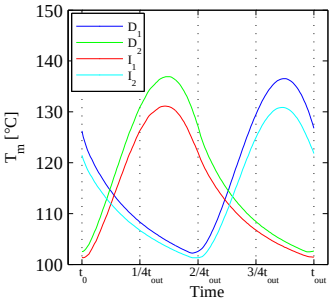
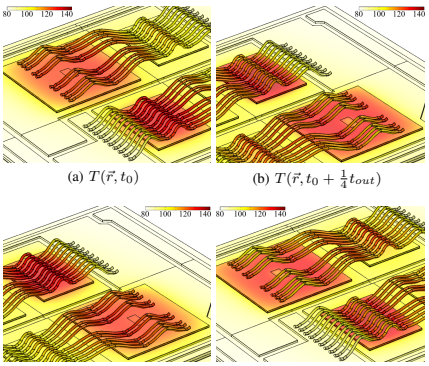


Fig. 6. Junction temperature of the four semiconductor components subjected to sinusoidal load conditions after reaching a steady cycle.

temperature distribution around the active components is presented at time t_0 and three time steps one fourth of the output time after: $t_0 + \frac{1}{4}t_{tout}$, $t_0 + \frac{2}{4}t_{tout}$, and $t_0 + \frac{3}{4}t_{tout}$. The time t_0 notes the beginning of a power cycle after the mean junction temperatures T_m of the different chips have reached a steady cycle. The sinusoidal load is naturally at it's peak for I_1 and D_2 at $\frac{1}{4}t_{tout}$ and I_2 and D_1 at $\frac{3}{4}t_{tout}$. However, as presented in Fig. 6 the junction temperatures are still increasing after the peak power loss has been reached. This is due to the power loss still being higher than the outward flux due to water and passive cooling.

3) Section Temperature: Fig. 7 shows a clear tendency of uneven temperature fields across the surface of the chips as reported on numerous occasions, see [12], [14], [16]. However, the majority of these results were obtained without including bond wires in the actual thermal simulations. The



(a) $T(\vec{r}, t_0)$ (b) $T(\vec{r}, t_0 + \frac{1}{4}t_{out})$

(c) $T(\vec{r}, t_0 + \frac{2}{4}t_{out})$ (d) $T(\vec{r}, t_0 + \frac{3}{4}t_{out})$

Fig. 7. Temperature surface plots of the active elements at selected points during one power cycle after reaching a stable mean junction temperature.

difference observed by including the bond wires on this particular geometry is significant. Power loss on both LS and HS chips are initially identical, however, due to the bond wires the LS and HS diode are not experiencing the same thermal reservoir. This is also visible in Fig. 2b were the Cu pad beneath the Al wire connection to the DCB is of noticeable less volume.

B. Simplified Degradation Model

From $T_m(t)$ in Fig. 6 a quick simplified simulation of the degradation function $D(\vec{r}, t)$ in a given region can be carried out. As presented in Fig. 1 the simulation of $D(\vec{r}, t)$ requires the plastic strain as input. Accordingly, an analytical equation is needed which, as discussed in Sec. IV-C, can be done from a 1D assumption. Furthermore, a specific geometry needs to be specified for the degradation evaluation. From [16] it was clear that bond wire related issues was the primary concern, accordingly, a typical wire end bond is regarded. In Fig. 8 the peak degradation value (near the heel) is plotted against time for identical bond wire interfaces placed on the four chips.

In the accelerated test the diodes are supposed to be stressed most severely, which is clearly seen in Fig. 8. Furthermore, as discussed in Sec. V-A, the LS components are experiencing a higher ΔT than the HS. This increased load is even more clear in this simplified degradation evaluation.

C. Detailed 3D Degradation Simulation

1) Plastic Strain Field: Based on the temperature field the thermo-mechanical analysis is carried out as described in Sec. IV-C. As mentioned in the section, material hardening is presently included in the degradation assessment, but not the strain calculation. In Figs. 9 surface plots of the increase in effective plastic strain de_p^e in two interfaces are plotted for a line across the interface for a full power cycle. The

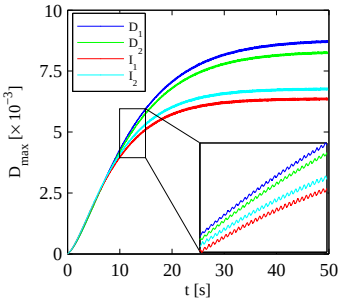
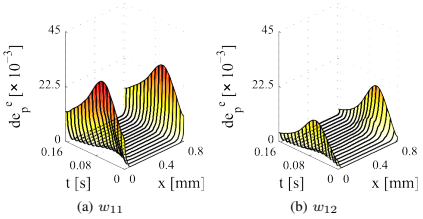


Fig. 8. Degradation evaluation near heel of end wire bond experiencing mean temperature as plotted in Fig. 6.

interfaces regarded are w_{11} and w_{12} which are illustrated in Fig. 2b. To limit the data presented only the effective plastic strain along a line from the beginning to the end of the bond is presented. The line is parallel to the wire curve placed in the center of the bond in the wire/metallization interface. To summarize, when following the plot along the first axes the spatial variation along the line is observed at a fixed time. Similarly, when moving along the second axes the time-resolved variation at a fixed position is observed. The motivation for plotting the change in effective plastic strain is to highlight the critical regions versus time.

As were expected de_p^e is highest near the heel and toe of

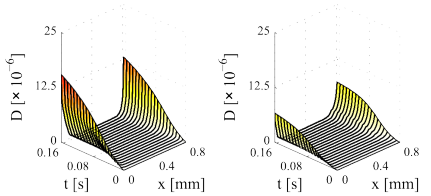


(a) w_{11} (b) w_{12}

Fig. 9. Effective plastic strain plotted along a line x, placed in the center of the wire bond, for a complete power cycle t_{out}.

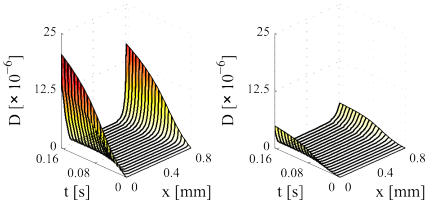
the interfaces and at the peak value of the local temperature. Heel and toe provide natural areas for crack propagation and are the main regions limiting expansion of the wire curvature. From the derived temperature field and effective plastic strain Eqs. (14)-(19) can be utilized for derivation of the degradation parameter $D(\vec{r}, t)$. In Figs. 10-14 surface plots of $D(\vec{r}, t)$ is presented in the same way as the effective plastic strain was in Figs. 9. The numbering in the figure captions is identical to the concept presented earlier, the initial number denote the wire and the second the interface. Keep in mind that the degradation parameter is a unitless quantity and as such the absolute value of it is only relevant when compared to other positions, times, or failure criteria.

A clear tendency of the fastest degradation of the first



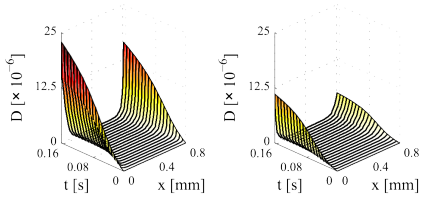
(a) w_{11} (b) w_{12}

Fig. 10. Degradation function of stitch bond (a) and end bond (b) of w_1.



(a) w_{21} (b) w_{22}

Fig. 11. Degradation function of stitch bond (a) and end bond (b) of w_2.

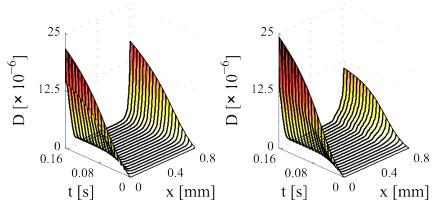


(a) w_{31} (b) w_{32}

Fig. 12. Degradation function of stitch bond (a) and end bond (b) of w_3.

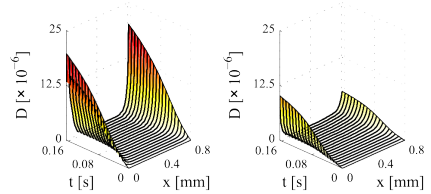
interface is observed in a majority of the images. Similarly, the degree of degradation is the largest near the beginning of the bond footprint. Finally, performing the same simulation for the remaining wire interfaces in the section indicates that specific interfaces and interface are degrading faster than the remaining. These can be divided into specific groups with some interfaces being in multiple groups. The enumeration is ordered after degree of damage in a rising manner:

1) Wire interfaces facing another chip, in this example $w_{11}, w_{21}, ..., w_{91}, w_{101}$.
2) Clustered interfaces, in this example w_{31}/w_{32} and w_{41}/w_{42}
3) Interfaces facing a wire curvature - end bonds are in general less damaged than stitch bonds.



(a) w_{41} (b) w_{42}

Fig. 13. Degradation function of stitch bond (a) and end bond (b) of w_4.



(a) w_{51} (b) w_{52}

Fig. 14. Degradation function of stitch bond (a) and end bond (b) of w_5.

VI. Discussion

From the simulated temperature fields, strain, and degradation function it is clear that the sample chosen to illustrate the modelling approach shows non-homogeneous wear in numerous ways: on module level with difference between sections, on section level with changing load between chips, and on chip level with differently affected wire bondings.

A. Parallel Sections in Power Modules

Calculation of the temperature field is the initial step to indicate problems in component design. In Fig. 2a a full module with six identical sections is illustrated. Even with a constant convection parameter and water-cooling temperature as a boundary condition the mean temperature of the DCB ceramic depends on the section position. This is a commonly reported problem, even with water-cooling systems, and in this case the temperature difference is not critical.

B. High and Low Side Configuration

In numerous applications the HS and LS problem with regard to active components is common. However, the present situation should not display such tendencies. The accelerated test setup was designed to apply a sinusoidal load similar to real life conditions with equally distributed power loss between similar components - which initially was the case. Over time, however, the LS diode displayed clear tendencies of increased stress - increase in forward voltage, and material

changes from visual inspection after testing, see [17] and [31], respectively. This problem was through the temperature simulation alone, see Fig. 6, identified to be directly related to local temperature. The thermal reservoir experienced by the LS diode chip is simply not identical to the HS. As is clear from the degradation calculations this also accelerates the degradation of the interconnects, as indicated in the mean degradation parameter in Fig. 8. Temperature differences in between chips are, however, more critical. The accelerated test is designed to stress and damage the freewheeling diodes and this is also clear from the junction temperature plotted in 6. Initially, the powerloss is identical in the HS and LS components which is also supported by measurements of the forward voltage in [16]. However, over time the forward voltage is observed to increase steadily on the LS diode (D_2) which is consistent with thermal simulations - forward voltage is temperature dependent.

C. Bond Wire Degradation

Non-homogeneous temperature distributions on the chip level is in the same way as on the module level a common problem. The center of the chip experience a higher thermal impedance than the edge of the chips resulting in additional heating. This creates a tendency of faster material degradation near the center wire bonds compared to edge bonds.

The observed degradation behaviour is to some degree consistent with experimental data. In general the LS diode in this geometry under these load conditions have been reported on several occasions to be the failing part, see [17], [31], [32]. However, separating the individual wire bonds from each other is only carried out in [32]. On the diodes a tendency of center wire bonds to be degrading faster is clear, however, the variation in production seems to overpower the difference in wire bond position with regard to comparing individual bonds. This could be handled by inspecting additional samples. Regarding the first group presented in Sec. V-C a clear tendency with lifted wires is that bonds facing another chip are more inclined to fail, see [31].

D. Fracture Analysis and Change in Electrical Parameters

The next step in this degradation evaluation would be to derive the fracture speed from the degradation function. In Fig. 8 one would specify a parameter D_{FC} as a fracture criteria and as a plane in Figs. 10-14. When $D(\vec{r},t) > D_{FC}$ the region would be marked as fractured. The main approach for specifying the fracture criteria D_{FC} would be through experimental investigation of interface degradation using four-point probing. However, as mentioned above additional data is needed.

From the mapping of the fracture parameter, however, it would be possible to plot the change in effective resistance of the individual bond wires through the method in V-C and a mean wire bond from Sec. V-B. This would enable either a very clear image of the module wear-out process or an approach for end-of-life assessment.

VII. Conclusion

A detailed 3D modelling approach for simulation of thermo-mechanical degradation of interconnects in high power IGBT modules is presented. The model allows for simplifications speeding up the simulation process for end-of-life estimation as well as detailed mapping of the degradation distribution on individual wire level.

The model is built in a structured manner allowing for simulation of individual elements like power loss, temperature fields, mechanical analysis, and material degradation, see Fig. 1. By separating these steps on an acceptable level it is possible to initiate the model at any level by simply supplying the previous one as an external load. This allows for a stepwise increase in model detail to ensure the right information in the end. Presently, this has been utilized in many ways. The effect of the position of the individual sections on the baseplate is handled only in the thermal analysis. Similarly, the plastic strain field calculation, which is very time consuming, is limited in 3D to specific wire bonds and on the large scale derived from a simplified 1D slab model.

By applying the model to a specific case, a high power IGBT module subjected to a sinusoidal load under accelerated conditions, an image of the possibilities is outlined. From the thermal analysis design problems were found at both the module, section, and chip level - see Section V-A. While the module level distribution issues are common, and limited in the present situation, the section problem between LS and HS components is substantial. In Fig. 6 the average junction temperature is plotted for the four semiconductor components and while the difference on this scale seems marginal the difference in degradation speed is more pronounced, see Fig. 8. This problem is also consistent with experimental results as presented in [16], [31].

Similar to the module level distribution issue, the temperature distribution on a power transistor or diode is commonly known. Wires placed near the center of a chip often delaminate or lift-off sooner than edge wires. This is also illustrated in Figs. 10-14 with the presented degradation fields, however, additional groupings of higher stressed bonds are possible. Wires closer to other active components are more stressed due to additional heating, and edge bonds are stronger than stitch bondings due to lack of wire curvature. All in all this illustrates the inadequacy of the commonly used lifetime estimation methods based on a standard CM or CM-A approach, and highlight the necessity of new more detailed multiphysics based approaches.

Acknowledgment

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References

[1] J. M. Guerrero, F. Blaabjerg, T. Zhelev, K. Hemmes, E. Monmasson, S. Jeme, M. P. Comech, R. Granadino, and J. I. Frau, "Distributed generation," *IEEE Industrial Electronics Magazine*, vol. 4, pp. 52–64, 2010.

[2] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, pp. 653–667, 2002.
[3] U.Scheuermann and U.Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," *PCIM Nuremberg*, pp. 59–64, 2002.
[4] C. Hager, Y. Tronel, and W. Fichtner, "Electro-thermo-mechanical simulations of aluminum bond wires in IGBT-packages," *Technical Proceedings of the 1998 International Conference on Modelling and Simulation of Microsystems*, pp. 163–167, 1998.
[5] W. Kanert, "Active cycling reliability of power devices: Expectations and limitations," *Microelectronics Reliability*, vol. 52, pp. 2336–2341, 2012.
[6] O. Schilling, M. Schfer, K. Mainka, M. Thoben, and F. Sauerland, "Power cycling testing and fe modelling focussed on Al wire bond fatigue in high power IGBT modules," *Microelectronics Reliability*, vol. 52, pp. 2347–2352, 2012.
[7] J. Lutz, U. Scheuermann, H. Schlangenotto, and R. D. Doncker, *Semiconductor Power Devices - Physcis, Characteristics, Reliability*. Springer-Verlag, 2011, ISBN: 978-3-642-11124-2.
[8] L. Yang, P. A. Agyakwa, and C. M. Johnson, "Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules," *IEEE Transactions on Device and Materials Reliability*, vol. 13, pp. 9–17, 2013.
[9] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, T. Abeyasekera, and P. Rodriguez, "An overview of the reliability prediction related aspects of high power IGBTs in wind power applications," *Microelectronics Reliability*, vol. 51, pp. 1903–1907, 2011.
[10] U. Scheuermann and R. Schmidt, "A new lifetime model for advanced power modules with sintered chips and optimized Al wire bonds," in *Proceedings of PCIM Europe*, 2013, pp. 810–817.
[11] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test for IGBT modules in traction application," *Power Electronics and Drive Systems*, pp. 425–430, 1997.
[12] B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, and M. Thoben, "Thermo-mechanical analysis of bonding wires in IGBT modules under operating conditions," *Microelectronics Reliability*, vol. 52, pp. 2353–2357, 2012.
[13] K. B. Pedersen, P. K. Kristensen, V. Popok, and K. Pedersen, "Interface structure and strength of ultrasonically wedge bonded heavy aluminium wires in Si-based power modules," *Journal of Materials Science: Materials in Electronics*, vol. 25, no. 7, pp. 2863–2871, July 2014.
[14] S. Filippis, H. Köck, M. Nelhiebel, V. Kosel, S. Decker, M. Glavanovics, and A. Irace, "Modelling of highly anisotropic microstructures for electro-thermal simulations of power semiconductor devices," *Microelectronics Reliability*, vol. 52, pp. 2374–2379, 2012.
[15] U. Scheuermann and R. Schmidt, "Impact of load pulse duration on power cycling lifetime of Al wire bonds," *Microelectronics Reliability*, vol. 53, pp. 1687–1691, 2013.
[16] P. Ghimire, K. B. Pedersen, A. R. de Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thøgersen, "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application," in *Proceesings of the 8th International Conference on Integrated Power Electronic Systems*, 2014, ISBN: 978-3-8007-3578-5.
[17] P. Ghimire, K. B. Pedersen, B. Rannestad, A. R. de Vega, S. Munk-Nielsen, and P. B. Thøgersen, "Real time wear-out monitoring test setup for high power IGBT modules under sinusoidal loading condition," *Submitted to IEEE Transactions on Power Electronics*, 2014.
[18] K. Olesen, R. Bredtmann, and R. Eisele, ""ShowerPower" new cooling concept for automotive applications," in *Proceedings of the Automotive Power Electronics*, 2006.
[19] M. H. Bierhoff and F. W. Fuchs, "Semiconductor losses in voltage source and current source IGBT converters based on analytical deriviation," in *35th Annual Power Electronics Specialties Conference*, 2004, pp. 2836–2842.
[20] A. D. Rajapakse, A. M. Gole, and P. L. Wilson, "Approximate loss formulae for estimation of IGBT switching losses through emtp-type simulations." IEEE, 2005.
[21] A. Wintrich, U. Nicolai, W. Tursky, and T. Reimann, *Application Manual Power Semiconductors*. SEMIKRON International GmbH, 2011, ISBN: 978-3-938843-66-6.
[22] M. A. Bhatti, *Fundamental Finite Element Analysis and Applications*. John Wiley & Sons, 2005, ISBN: 0-471-64808-6.
[23] R. Codina, "Comparison of some finite element methods for solving the diffusion-convection-reaction equation," *Computer Methods in Applied Mechanics and Engineering*, vol. 156, pp. 185–210, 1998.
[24] F. P. Incropera, D. P. Dewitt, T. L. Bergman, and A. S. Lavine, *Fundamentals of Heat and Mass Transfer*. John Wiley & Sons, 2007, ISBN: 978-0-471-45728-2.
[25] A. Bejan and A. D. Kraus, *Heat Transfer Handbook*. Wiley and Sons, 2003.
[26] M. Ashegi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, "Thermal conduction in doped single-crystal silicon films," *Journal of Applied Physics*, vol. 91, pp. 5079–5088, 2002.
[27] J. Goehre, M. Schneider-Ramelov, U. Geißler, and K. Lang, "Interface degradation of Al heavy wire bonds on power semiconductors during active power cycling measured by the shear test," in *Proceedings on Integrated Power Electronics Systems*, no. 3.4, 2010, ISBN: 978-3-8007-3212-8.
[28] C. Hager, "Lifetime estimation of aluminum wire bonds based on computational plasticity," Ph.D. dissertation, Swiss Federal Institute of Technology, 2000.
[29] K. B. Pedersen, P. K. Kristensen, V. Popok, and K. Pedersen, "Degradation assessment in IGBT modules using four-point probing approach," *IEEE Transactions on Power Electronics*, 2014, in press - DOI: 10.1109/TPEL.2014.2344174.
[30] L. Yang, P. A. Agyakwa, and C. M. Johnson, "A time-domain physics-of-failure model for the lifetime prediction of wire bond interconnects," *Microelectronics Reliability*, vol. 51, pp. 1882–1886, 2011.
[31] A. R. de Vega, P. Ghimire, K. B. Pedersen, I. Trintis, S. Beczckowski, S. Munk-Nielsen, B. Rannestad, and P. B. Thøgersen, "Test setup for accelerated test of high power IGBT modules with online monitoring of Vce and Vf voltage during converter operation," in *Proceedings of the International Power Electronics Conference*, 2014, pp. 2547–2553.
[32] K. B. Pedersen, L. H. Østergaard, P. Ghimire, V. Popok, and K. Pedersen, "Degradation mapping in high power IGBT modules using four-point probing," 2014, submitted to: Microelectronics Reliability.

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PAPER G

Degradation mapping in high power IGBT modules using four-point probing

Degradation Mapping in High Power IGBT Modules using Four-Point Probing

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Abstract

An electrical four-point probing approach is used to estimate local degradation in high power insulated gate bipolar transistor modules subjected to active thermal cycling. By measuring electrical parameters of selected units and components the possibility of mapping the degradation is demonstrated. The development of failures is put in accordance with physical phenomena and materials fatigue. These results are directly usable for reliability purposes with a focus on geometry optimization and enhanced lifetime prediction methods.

Keywords: Degradation distribution and evolution, four-point probing, bond wire lift-off, metallization reconstruction

1. Introduction

Power devices are essential parts in a large variety of application fields including energy generation, consumer-, and automotive electronics. In all mentioned fields reliable devices are a key feature in order to prevent early device failures. Especially, in high power application fields reliability is a key issue since failure of devices operating at high currents and voltages may seriously damage surrounding systems. As the loads on power devices is growing the need for proper reliability design based on detailed knowledge of the physics behind failures increases. [1, 2, 3]

In modern power modules pulsed load conditions with high currents and fast switching is a common situation. Temperature fields generated by electrical pulses have large fluctuations and gradients across the different layers constituting the electronic unit. Oscillations in temperature are a well-known source of thermo-mechanical stress caused by material expansion[4], and a difference in the coefficients of thermal expansion (CTE) for various materials [5, 6]. Similarly, large temperature gradients cause local stresses due to differences in CTE of materials[7]. Finally, oscillations at high average temperatures are a known source of metallization reconstruction[2, 3].

Modelling the lifetime of a power module subjected to thermal cycling has been of interest for many years. Approaches have varied from more or less advanced statistical models [5, 6, 8, 9] to physics-of-failure based approaches [10, 11, 12]. Mapping the degradation distribution and evolution inside the insulated gate bipolar transistor (IGBT) modules not only yields the possibility of enhancing the presently used lifetime estimation methods, but also to assess the quality of the component layout.[13]

Typically, failure and degradation investigations are catastrophically damaging processes, destroying the component of interest[14, 15]. However, four-point probing presents a low current measurement method with negligibly small mechanical impact from the probes and with no additional thermal stress. Based on this, it is possible to carry out the characterization and then place the module back into operation. In the future this could be an approach for understanding on-line monitoring results, e.g. like changes in the forward voltage[16].

In the current paper the change in device performance is investigated as a function of time for a high power IGBT module subjected to power cycling (commonly referred to as active thermal cycling as well). By applying four-point probing a change in electrical parameters of different components and units is monitored that allows a mapping of the degradation distribution which is used directly to assess the source of a potential early failure. The results of electrical characterization are compared with the microscopy-based investigations to ensure validity of

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the results obtained by the four-point probing and to provide physical picture and origins of the degradations.

2. Samples

The investigated sample is a high power 1700V/1000A IGBT module consisting of six identical sections. Each section is composed of two IGBT chips, two free-wheeling diodes, and 20 heavy Al bond wires, see Fig. 1. Sections are numbered from 1-6 (S_{1-6}) starting at the section closest to the module gate terminal. The wires are numbered from 1-10 (w_{1-10}) starting at the position closest to the section edge and moving inwards. The vertical layer geometry is presented in Table 1.

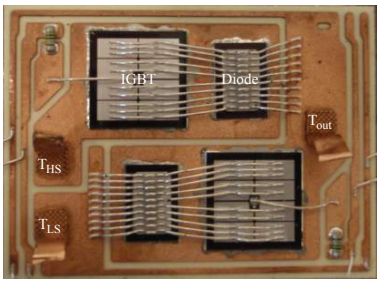


Figure 1: Image of a single section of the IGBT module. HS and LS denotes which side would be the high and low side in the section if placed in the power cycling setup. T denotes the section terminals.

Table 1: IGBT module vertical layer layout.

Layer - Material	**Thickness** [μm]
Bond wire - Al	400
Metallization - Al	6
Chips - IGBT/diode	200
Solder - $SnAg$ 96.5%/3.5%	100
DCB - $Cu/Al_2O_3/Cu$	300/380/300
Solder - $SnAg$ 96.5%/3.5%	100
Baseplate - Cu	3000

3. Methods

The samples are stressed using a power cycling (accelerated test) setup and then investigated using four-point probing. Both methods are described in detail in [17] and [13], respectively. To verify the relation between the change of electrical parameters and degradation as well as failure mechanisms a few selected studies of the metallization and the wire/chip interfaces were carried out using scanning electron microscopy (SEM) and micro-sectioning approach combined with optical microscopy [15].

3.1. Power Cycling

A standard H-bridge topology with the device under test (DUT) placed on one leg and the control units on the other is used as a power cycling setup. The control side delivers a sinusoidal current load to the DUT with a fundamental frequency (f_{out}) of $6Hz$ and a peak current (I_{tot}) of $922A$. Meanwhile the IGBT switching frequency (f_{sw}) is maintained at $2.5kHz$ under a DC link voltage of $1000V$. The test setup is designed to simulate field conditions of a wind power converter. All load parameters are kept close to realistic operating regime at an accelerated level to obtain device degradation. The setup is described in detail in [16, 17, 18].

Six modules are subjected to a different number of cycles, see Table 2. The modules were removed from the power cycling setup at selected number of power cycles corresponding to the estimated lifetime. As described in [18] this is done by monitoring the changes in the forward voltage. The observed increase in the voltage due to module wear-out is also one of the motivations for the four-point measurements as it could single out the primary degrading elements.

The subscripts in the sample numbering in Table 2 denote the approximate state in the lifetime curve. $F_{100\%}$ represents sample run until catastrophic failure. Sample $B_{25\%}$ is tagged because it was stressed under different conditions than the remaining samples. All power cycling parameters were the same, however, the temperature of the cooling water was not monitored during operation and early changes in the on-state voltage were observed. Therefore, this sample is

Table 2: IGBT module samples regarded.

Name	**# cycles** [$\times 10^6$]
A_{New}	0
$B_{25\%}$	1.3*
$C_{50\%}$	2.5
$D_{70\%}$	3.5
$E_{90\%}$	4.5
$F_{100\%}$	5.1

not directly comparable to other samples. The main reason for investigating the sample is to identify a potential cause of early degradation under the given test conditions.

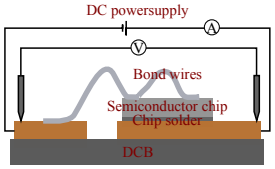
3.2. Four-Point Probing

Four-point probing is commonly used for measuring electrical properties of semiconductor chips, as well as fracturing or degradation in various conducting structures [13, 19, 20]. The concept is based on having two current carrying terminals attached to the sample while placing two probes in between for measuring the potential difference across the region of interest. This method eliminates any resistance contributions from the probe and enables high resolution measurements of the local resistance.

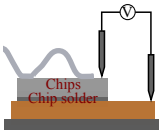
All measurements are performed by applying a current from 0 to 5A in steps of 0.4A to the section terminals. The relatively low current is chosen to limit electro-thermal heating of the samples. The sample temperature is controlled by Peltier elements combined with a data acquisition card and software based on the proportional-integral-derivative (PID) approach. PID is a commonly applied algorithm for controlling e.g. the temperature in a system from a signal control loop. The measurements are carried out using tungsten probes designed for electrical investigations and attached to μm resolution XYZ stages allowing high precision in the positioning. The details of the entire setup and concept are presented in [13].

The different measurement schemes are illustrated in Figs. 2a-c. Fig. 2a illustrates the first scheme utilized where the potential difference is measured between the terminals. According to the section illustrated in Fig. 1 one can carry out the measurements on the HS and LS IGBT and the equivalent free-wheeling diodes. Terminal measurements yield a very quick image of the general state of either IGBT or diode. Furthermore, it allows identification of changes as being either interconnect- or semiconductor-related. The former would appear as a change of an ohmic type while the latter would affect the IV curve of the semiconductor.

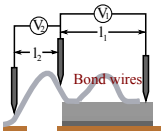
Besides the general state of the section the different interconnects and components can be studied. This is illustrated in Figs. 2b and 2c. The solder is always reached through the semiconductor chips, thus, reducing the resolution of the measurements. Furthermore, the connection to the chip goes through the metallization, making it necessary to perform several measurements to exclude contributions from metallization changes. Measurements on bond wires



(a) Placement of current carrying wires and probes positioning on the section terminals.



(b) Measurements across metallization, semiconductor chips, and solder.



(c) Bond wire measurements.

Figure 2: Illustration of the different probing configurations.

are easier realized compared to the solder. By measuring the potential difference on top of the wire curve (V_2) over a fixed and known distance (l_2), as shown in Fig. 2c, the local current can be deduced in each wire, for details see [13]. Using the local current together with the potential difference across the wire connections (V_1) with the fixed distance (l_1), the effective interface resistance is obtained.

3.3. Microscopy Based Investigations

The electro-thermal degradation of the interconnects is investigated using different microscopy based methods. Metallization reconstruction is characterized using a Zeiss 1540 XB SEM/FIB. The wire/chip interfaces are studied using a micro-sectioning approach combined with optical microscopy. This yields cross-sectional views of the wire bonds. Both techniques are described in detail in [21].

4. Results

4.1. Initial Observations

Prior to the four-point probing measurements standard visual inspections of the modules are performed. The observations revealed wire lift-off which is found to be the dominating failure for LS diodes (see Table III). This tendency is consistent with the change in forward

voltage measured during the power cycling presented in [16].

Table 3: Wire lift-off in IGBT modules.

Module	Section	Observations
A_{New}	-	-
$B_{25\%}$	S_1 LS	w_5 is lifted off
$C_{50\%}$	-	-
$D_{70\%}$	S_1 HS	One bond of $w_{1,8}$ and both of w_{2-7} are lifted off.
	S_3 LS	One bond of $w_{1,6,7}$ and both of w_{8-10} are lifted off.
	S_4 LS	One bond of w_{8-10} is lifted off.
$E_{90\%}$	-	-
$F_{100\%}$	-	Blown up

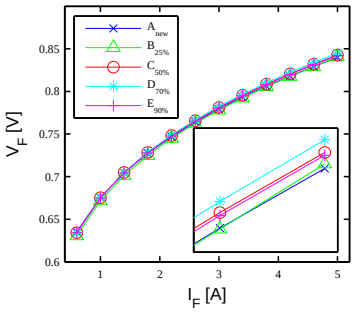
4.2. Four-Point Probing

The four-point probing approach was applied to selected sections of all modules. From these measurements, it was clearly observed that the HS and LS of the modules are damaged differently. This is in accordance with the simulated medium value (T_m) and amplitude (ΔT) of the temperature field experienced by the HS and LS which are presented in [22]. There it is shown that the bond wires' connections to the Cu pads create a difference in thermal impedance of LS and HS components. This causes a small increase in ΔT for the LS components thereby leading to increased stress. These simulated results are consistent with the increased damage observed on LS diodes. Based on this, additional measurements are carried out for the selected samples.

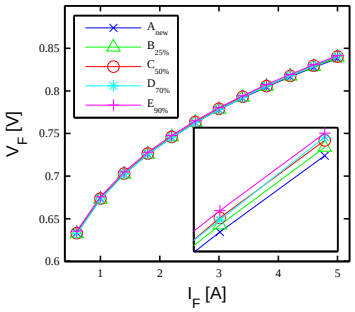
4.2.1. Terminal Measurements

In Fig. 3 the mean forward voltage as a function of applied current for the LS and HS diodes, respectively, is presented.

A small increment in the mean forward voltage with number of power cycles can be seen in the inserts to both panels. For the HS diodes this increment appears to be proportional to the number of cycles, whereas for the LS diodes the increments depends randomly on the number of power cycles with module $D_{70\%}$ showing the highest forward voltage. In order to understand these dependences one needs to remember that the



(a) LS diodes.



(b) HS diodes.

Figure 3: Dependence of mean forward voltage on current between the terminals for (a) LS and (b) HS diodes of new and cycled modules. Mean voltages for LS diodes are obtained through the averaging on all sections for every module. Mean voltages for HS diodes are obtained through the averaging on a few selected sections for every module. Inserts to both panels show the voltage measurements for currents of 4.6 and 5.0 A.

measurements involve metal components, semiconductor chip and several interfaces. The change due to bond wire fracturing, solder creep or metallization reconstruction can be expected on the scale of mV whereas the diode forward voltage at $50°C$ and $5A$ is around $0.8V$. Temperature variations should also be considered, and while the mean section temperature is controlled with the precision of $0.1°C$ the temperature field across the chip might vary on a higher level, thus, affecting the forward voltage. Therefore, one cannot expect distinguishable degradation picture of individual

interconnections when measuring on entire section.

4.2.2. *Measurements through metallization, semiconductor chip and solder*

To reduce the number of involved components, the measurement between terminals was divided into two: firstly, from a terminal to the chip surface through the semiconductor chip, and secondly through the wires. This approach helps to isolate the chips and wires from each other and, thus, find the location of the main contributor to the degradation.

In Fig. 4 differential voltage as a function of current is presented for all modules. The differential voltage is calculated by subtraction of the voltage measured on the new module from that obtained for the cycled one. Measurements are performed from chip surface through the diode to T_{HS}/T_{out} for the HS and LS diodes, respectively, as illustrated in Fig. 2b. To ensure reliability of the measurements they were repeated for different probe positions on the metallization. The maximum observed variation in this measurement approach on the diodes for a new component was $2.68mV$. Therefore $\Delta V_F = \pm 1.34mV$ is considered to be within production variation. The obtained dependences show clear difference between the new and cycled modules, with parameters of many samples outside the production variation. If one excludes curves for module $B_{25\%}$ from the analysis (due to the reason mentioned in section 4.1) it can be concluded that ΔV gradually increases with the number of cycles for HS diodes. There is also increase of ΔV for LS diodes but the maximal value is observed for module $C_{50\%}$. The fact that $C_{50\%}$ displays the highest degree of degradation is not accredited to be of significant importance because the value is small and as will be shown later the metallization degradation is a minor problem compared to the wire lift-off.

The observed rise of ΔV with increased power load can be related to either solder degradation, metallization reconstruction, or variation in the semiconductor chips. More studies are required to distinguish between contributions of these three possible degradation mechanisms.

4.2.3. *Measurements on Bonded Wires*

To investigate the wire degradation the current distribution between the ten wires on each chip was measured for every section of each module using the configuration described in section 3.2 and shown in Fig. 2c. It was found that the current varies from wire to wire on both types of semiconductor chips, namely on the diodes and IGBTs. The obtained dependences of mean fractional

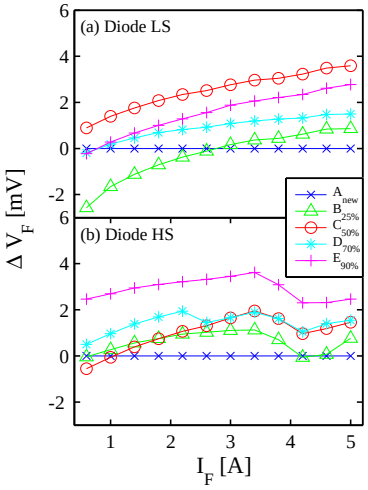


Figure 4: Differential voltage as function of current measured from terminal to metallization for the (a) LS and (b) HS diodes.

currents are presented in Figs. 5 and 6, the variation in measurement technique is discussed in detail in [13]. For the diodes the current is nearly equally distributed except for the outermost (edge) wires, see Figs. 5a and 5b. Nearly equal currents running through $w_{2\text{–}9}$ can be explained by the exactly equal distances between the bonded wires while $w_{1,10}$ located at the edges can posses slightly larger surface areas thus providing conditions for higher local currents. It is observed that for the HS diodes the current distributions for the stressed modules are very similar to that of the new module except for the $D_{70\%}$. However, if one removes the current values of S_1 from the $D_{70\%}$ distribution, then the curve coincides very well with the new module curve. The large effect on the mean current distribution in $D_{70\%}$ from S_1 is due to the lifted wires that is specified in Table 3. For the LS the current distributions for the wires of the stressed modules differ significantly from those of the new module. This indicates that there is a significant degradation of the wires or wire bonds of the LS diodes.

For the IGBTs it is observed that the current distribution follows the spacing of the wires on the metallization surface as shown in Fig. 1. One can split the wires into two groups: edge located (1-3 and 8-10) and center (4-7). It is seen in Fig. 6 that the central wires ex-

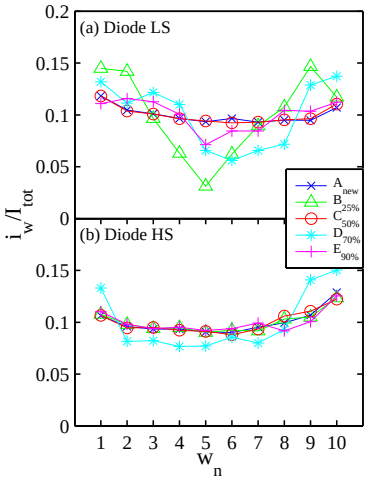


Figure 5: The current distribution for the LS and HS diode bond wires. First axis shows wire numbering as explained in section 2. Second axis presents fractional current, i.e. the ratio of the current going through the wire to the total current applied to the device. The lines connecting the experimental dots are presented only for visual guidance.

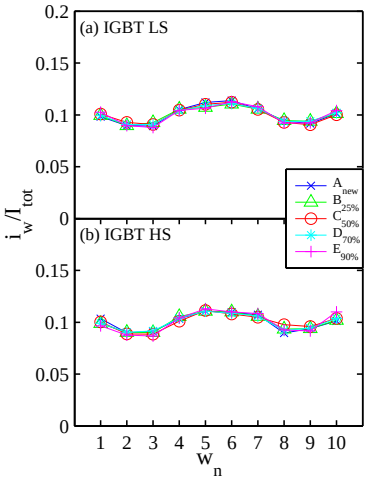


Figure 6: The current distribution for the LS and HS IGBT bond wires. First axis shows wire numbering as explained in section 2. Second axis presents fractional current, i.e. the ratio of the current going through the wire to the total current applied to the device. The lines connecting the experimental dots are presented only for visual guidance.

hibit slightly higher fractional current for both LS and HS IGBT. Contrary to the LS diodes, the current distribution through the IGBT wires does not change with increasing number of power cycles.

4.2.4. Resistance of Wire Bonds

Resistance through the wire bonds is measured for both the diodes and IGBTs. The obtained dependences of effective resistance (difference in resistance between the cycled and new module for the given wire) are shown in Figs. 7 and 8 for the diodes and IGBTs, respectively. It is observed that the wire resistance of the stressed modules for both the diodes and IGBT's has a small increase (on the scale of $m\Omega$) compared to the new module except for the LS diodes (see Fig. 7a). S_1 of module $D_{70\%}$ was excluded from the analysis of the HS diodes due to the visually observed numerous wire lift-off. For the LS diodes the increase in resistance for the stressed modules is significant, especially for the central wires. It is necessary to mention that the increase of ΔR for LS diodes of module $D_{70\%}$ is mostly related to S_3 which gives a few times higher values compared to other sections. Therefore, the dependence for module $D_{70\%}$ is presented without S_3 and the data for this section are shown separately. For the HS diodes, $C_{50\%}$ shows higher wear of wire bonds with number of cycles compared to other samples. However, as follows from the dependences presented in Figs. 5b and 7b, the degradation is very similar to all wires, i.e. almost independent of the bond location on the chip.

4.2.5. SEM Investigation of Metallization

In Fig. 9 SEM images of the chip metallizations are presented. Figs. 9a and 9b are surface images of the diode and IGBT chip metallization from A_{New}. Figs. 9c and 9d are similar but for $E_{90\%}$.

By comparing Figs. 9a and 9c, it is clear that the metallization layer on the diode surface undergoes strong reconstruction. Reconstruction effects were observed on both HS and LS diodes with no visual difference. Focused ion beam milling was carried out on a couple of selected samples to investigate the

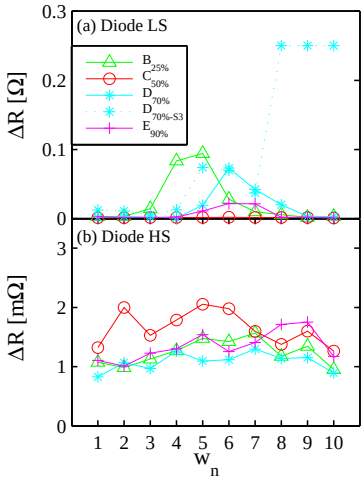


Figure 7: Change in effective resistance for the LS and HS diode bond wires of power modules subjected to different number of power cycles. Values above 0.25Ω are cut-off to ease the plot. S_1 has been excluded from the $D_{70\%}$ HS diodes. ΔR of LS diode of S_3 is presented separately.

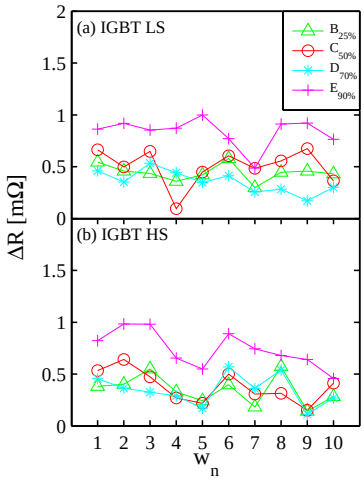


Figure 8: Change in effective resistance for the LS and HS IGBT bond wires of power modules subjected to different number of power cycles.

change in the layer structure with depth. It appears that the structure mostly changes in the topmost $1-3\mu m$ *Al* layer of the metallization, however, sometimes the reconstruction propagates down to the surface of the semiconductor chip through the entire metallization layer. Furthermore, in all samples there is an increased degree of degradation found at the chip center compared to the edges. The IGBT metallization appears to be unchanged with increase of number of cycles as can be seen from comparison of Fig. 9b and 9d.

4.2.6. Microscopy of Bond Wire Cross-Sections

In Figs. 10 and 11 cross-sectional images of bond wire/IGBT interfaces are presented for selected wires of samples $C_{50\%}$ and $E_{90\%}$.

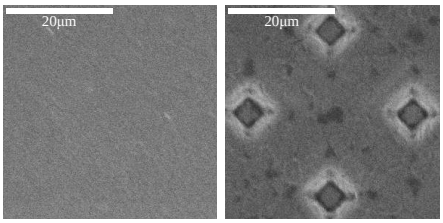
In both figures the bond wire lift-off process is clearly observed at different stages. In both cases the fracturing occurs close to the wire/chip interface which is attributed to the large granular structure, see [21]. In Fig. 10 the majority of the wire is still connected and the fracture is observed to move either below or inside the grains in the bottom of the interface. A similar picture is found in Fig. 11 for the module with much higher number of power cycles. In this particular cross-sectional view the wire is almost lifted off the chip, and the fracture is observed to either move between the grains or through them. As SEM and micro-sectioning studies are not the focus of this work, only a few selected images are presented to verify the concept of the four-point probing as degradation mapping approach.

5. Discussion

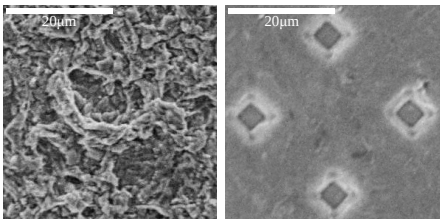
From the presented figures it is clear that the modules subjected to power cycling are, as expected, showing considerable wear. The observed wear can be divided into soft and hard degradation mechanisms.

5.1. LS Diode Failure

The current distribution between the LS diode bond wires in Fig. 5a displays a large change from A_{New} to the modules subjected to power cycling. This change indicates a non-homogeneous degradation process, i.e.



(a) A_{New} diode. (b) A_{New} IGBT.



(c) $E_{90\%}$ diode. (d) $E_{90\%}$ IGBT.

Figure 9: SEM images of the diode and IGBT metallizations for samples A_{New} and $E_{90\%}$.

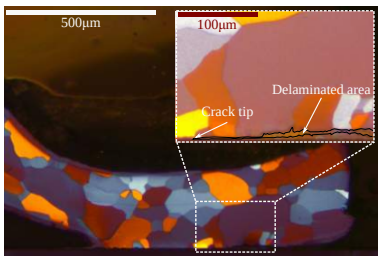


Figure 10: Bond wire/IGBT interface of $C_{50\%}$ sample. Lines are added to highlight the fracture area.

degradation of specific bonded wires on the LS diodes. If the bond wires degraded equally, the current distribution would remain close to constant with increase of the number of cycles. The hard wear-out is primarily experienced by the LS diode interconnections and results in the wire lift-off. This can be observed visually without electronic or microscopy based methods as explained briefly in Sec. 4.1. Taking into account the numerous wire lift-offs the higher degradation of LS diodes compared to other units becomes clear.

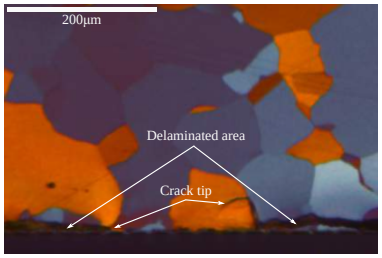


Figure 11: Bond wire/IGBT interface of $E_{90\%}$ sample.

Similarly, when regarding the change in effective resistance of the individual bond wires, wire lift-off effects are clear. While Figs. 7b, 8a, and 8b display changes on the scale of $m\Omega$ the resistance increase for LS diode in Fig. 7a is on the scale of Ω. In particular S_3 of $D_{70\%}$, which has been singled out, shows high wear on selected wires. Metallization reconstruction was found to be very similar for LS and HS diodes hence the hard wear is suspected to be primarily linked to the bond wires. The highly increased wear of specific wires is suspected to be related to the module production quality as single sections stand out, e.g. w_{8-10} of $D_{70\%}$ S_3 and w_5 of $B_{25\%}$ S_1.

5.2. *Fundamental Wear-Out*

If one excludes from the analysis the cases of significant change of the measured electrical parameters which are related to hard degradation mechanisms like the wire lift-off discussed above for the LS diodes, the fundamental wear-out or so-called soft degradation mechanisms can be studied. In Fig. 4b the change in forward voltage for the HS diodes is presented. Differential voltage increases with number of power cycles for a given current, hence, indicating the rise of resistance. This increase of resistance can be used as a measure of degradation which can be either related to a damaged solder or metallization reconstruction. The latter is clearly occurring as seen in Fig. 9c. However, similar change of ΔV was also found for IGBTs (not shown) but according to the SEM images (see Fig. 9b and 9d) the IGBT metallization does not undergo any considerable reconstruction. Therefore, the most probable mechanism of degradation would be the solder damage. On the other hand, more detailed study of the metallization reconstruction is required in order to support this conclusion.

From the current distributions presented in Figs. 5

and 6 it is observed that the local (fractional) currents through the wires are different due to the wire geometry and positioning on the chips. It is logical to suggest that the wires carrying higher currents will induce higher temperature variations at the corresponding interfaces with the metallization. This suggestion is supported by the simulations of the electro-thermal stresses. In [22] it is shown that under the power cycling the diode temperature field is higher in the chip center compared to the edges. This is a commonly observed problem in active chips being subjected to active thermal cycling, see [4]. Hence, bonds of w_{4-7} should experience higher thermal stresses and wear-out in the first place. The situation with IGBTs is different due to the presence of the gate terminal in the chip center. This leads to the formation of two high temperature areas off the central area. As a consequence w_5 and w_6 on the IGBTs experience lower ΔT compared to w_3 and w_7.

The dependences presented in Figs. 7 and 8 showing the increase in effective resistance for both diodes and IGBTs are in good agreement with the above-mentioned assumptions about fundamental wear-out or soft degradation of the bond interfaces. For the diodes, the bonds located close to the chip center degrade first which is indicated by the increase of the effective resistance with the number of power cycles. The increase can be explained by fracturing of the wire/metallization interfaces. This fractioning leads to the decrease of contact area, thus, causing an increase of the resistance. The increased wear observed in the $C_{50\%}$ wire bonds of the HS diode, displayed in Fig. 7b, is assumed to be within fundamental wear. However, this does not explain the increased degradation rate. No conclusive evidence is found in the micro-sectioning investigations of the samples. Thus, it can be suggested that the reason for the faster degradation of $C_{50\%}$ compared to $D_{70\%}$ and $E_{90\%}$ is the production quality.

The current distributions for all samples, presented in Figs. 6, show negligible small increase in fractional current with number of cycles. Dependences of effective resistance shown in 8 give better visualization of the differences. However, it is difficult to specify bonds degrading faster than others. The wire fractioning, which leads to the increase in effective resistance, is supported by the images presented in Figs. 10 and 11. To show precise relation between the change of electrical parameters and degradation mechanisms of particular units and components more investigations using SEM and micro-sectioning are required.

6. Conclusion

Five IGBT modules at different stages on a lifetime curve, from a new one to that close to failure, were studied using four-point probing electrical measurements in a few configurations. It is found that the measurements through the entire unit (terminal to terminal of the diode or IGBT) do not yield much of relevant information due to the fact that too many components are involved in the testing. Limiting the measurement to the metallization-chip-solder or bond wire configuration gives a possibility to localize the degradation to one or very few particular components or interfaces.

Typically, interconnection related failures are the most common in active power cycled devices and in the current study the four-point probing helped to indicate that the bond wire interfaces are the weakest points. The method allowed distinguishing between the highly accelerated (hard) and fundamental (soft) wear-outs related to the wire lift-off and fractioning of the wire/metallization interfaces, respectively. In particular, the study of LS diode bond wires showed good agreement between the electrical measurement, thermo-electrical simulations, visual and microscopy inspections, thus, allowing to give details on the degradation mechanisms. Finally, one can conclude that the four-point electrical probing method can be efficiently used for degradation assessment and mapping in high power IGBT modules. If this method is accompanied by microscopy techniques strong insights into particular degradation mechanisms and failures can be obtained which will be the subject of future study.

Acknowledgment

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References

[1] W. Kanert, Microelectronics Reliability 52 (2012) 2336–2341.
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, Application Manual Power Semiconductors, SEMIKRON International GmbH, 2011. ISBN: 978-3-938843-66-6.
[3] M. Ciappa, Microelectronics Reliability 42 (2002) 653–667.
[4] B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, M. Thoben, Microelectronics Reliability 52 (2012) 2353–2357.
[5] U. Scheuermann, R. Schmidt, Microelectronics Reliability 53 (2013) 1687–1691.
[6] M. Held, P. Jacob, G. Nicoletti, P. Scacco, M.-H. Poech, Power Electronics and Drive Systems (1997) 425–430.
[7] U. Scheuermann, R. Schmidt, in: Proceedings of PCIM Europe (2013), pp. 810–817.

[8] R. Amro, J. Lutz, in: Proceedings of IEEE Power Electronics Specialists Conference (2004), pp. 2593–2598.
[9] C. Busca, R. Teodorescu, F. Blaabjerg, S. Munk-Nielsen, L. Helle, T. Abeyasekera, P. Rodriguez, Microelectronics Reliability 51 (2011) 1903–1907.
[10] I. F. Kovačević, U. Drofenik, J. W. Kolar, in: Proceedings of the International Power Electronics Conference (2010), pp. 2106–2114.
[11] L. Yang, P. A. Agyakwa, C. M. Johnson, IEEE Transactions on Device and Materials Reliability 13 (2013) 9–17.
[12] L. Yang, P. A. Agyakwa, C. M. Johnson, Microelectronics Reliability 51 (2011) 1882–1886.
[13] K. B. Pedersen, P. K. Kristensen, V. Popok, K. Pedersen, IEEE Transactions on Power Electronics (2014). In press - DOI: 10.1109/TPEL.2014.2344174.
[14] J. Goehre, M. Schneider-Ramelov, U. Geißler, K. Lang, in: Proceedings on Integrated Power Electronics Systems (2010), 3.4. ISBN: 978-3-8007-3212-8.
[15] K. B. Pedersen, P. K. Kristensen, V. Popok, K. Pedersen, Microelectronics Reliability 53 (2013) 1422–1426.
[16] A. R. de Vega, P. Ghimire, K. B. Pedersen, I. Trintis, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P. B. Thøgersen, in: Proceedings of the International Power Electronics Conference (2014), pp. 2547–2553.
[17] P. Ghimire, K. B. Pedersen, A. R. de Vega, B. Rannestad, S. Munk-Nielsen, P. B. Thøgersen, in: Proceesings of the 8th International Conference on Integrated Power Electronic Systems. ISBN: 978-3-8007-3578-5.
[18] P. Ghimire, K. B. Pedersen, B. Rannestad, A. R. de Vega, S. Munk-Nielsen, P. B. Thøgersen, Submitted to IEEE Transactions on Power Electronics (2014).
[19] L. B. Valdes, Proceedings of the Institute of Radio Engineers (1954) 420–427.
[20] S. Pietranico, S. Lefebvre, S. Pommier, M. B. Bouaroudj, S. Bontemps, Microelectronics Reliability 51 (2011) 1824–1829.
[21] K. B. Pedersen, P. K. Kristensen, V. Popok, K. Pedersen, Journal of Materials Science: Materials in Electronics 25 (2014) 2863–2871.
[22] K. B. Pedersen, K. Pedersen, Submitted to IEEE Transactions on Power Electronics (2014).

PAPER H

Degradation evolution in high power IGBT modules subjected to sinusoidal current load

Degradation Evolution in High Power IGBT Modules subjected to Sinusoidal Current Load

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Abstract

In this paper the degradation evolution and distribution in high power IGBT module interconnects are investigated. Modules are subjected to advanced active thermal cycling by applying a sinusoidal current load switched actively by the device. A series of samples, subjected to an increasing number of power cycles under conditions resembling real life operation, are regarded. Primarily, bond wire lift-off and metallization reconstruction are observed in the module under the given loading. These mechanisms are investigated on a microscopic scale using micro-sectioning and scanning electron microscopy. The evolution and distribution is compared to the actual load conditions.

Keywords: Degradation distribution and evolution, micro-sectioning, bond wire lift-off, metallization reconstruction

1. Introduction

Power devices are today found in a large range of applications, from consumer electronics (battery chargers, mobile phones, etc.) to high power electronics (traction, automotive, electrical power transmission/distribution, etc.)[1]. Accordingly, the load experienced by a component varies significantly.

In high power modules, failures induced by power cycles are normally package related - meaning bond wire fatigue, metallization reconstruction, or solder fatigue[2, 3]. All three types of failures falls within low cycle fatigue - a low cyclic stress with progressive degradation over time leaving the device functional until catastrophic failure[4]. In common is the stress is induced by temperature variation and peak temperature. The difference in coefficient of thermal expansion (CTE) creates a stress between the interconnects and substrate and at a given level this stress is high enough to cause damage at an unacceptable rate.[5, 6]

Wire fatigue is normally divided into heel cracks and wire lift-off with the latter being dominant in later years[7]. Wire lift-off is created by fractures induced by thermal stress through CTE mismatch and wire flexure. Cracks are normally induced near the wire termination where the stress is highest due to limited expansion freedom. Especially, at the heel and toe of the wire bond where flexure is confined[3]. Lifting of a wire creates a domino effect, where initially a non-homogeneous current distribution is induced by the first lift. This increases the stress on surrounding wires causing additional lifts at an accelerated rate[4]. One often observes wire lifts in the forward voltage as small jumps[8].

Metallization reconstruction is a more gradual degradation process than wire lifting. As before mentioned it is primarily thermal related meaning reconstruction effects increases with temperature peak and variation[4]. Through recrystallization and extrusion of grains the *Al* metallization sheet resistance is increased over time. Additionally, in the end this may cause loss of contact to transistor cells or parts of a diode. Just before this a high current density causing melting or migration issues can occur thereby inducing other mechanisms[2]. Due to the gradual process of reconstruction, the sheet resistance increases slowly over time thereby affecting the forward voltage. However, metallization reconstruction are often observed as a part of general wear which means its affect on forward voltage is often shielded by increased chip temperature[9].

Solder fatigue is in contrast to wire lift-off and metallization reconstruction normally not affecting the forward voltage directly, due to size. Solder degradation generally affect the thermal impedance of the chip

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thereby causing an increased temperature load. The damage created is still a progressive phenomena induced by temperature variation, but the strain is more viscoplastic with creep and stress relaxation.[6]

In the present paper the degradation evolution of interconnects in high power IGBT modules subjected to a sinusoidal current load resembling real world conditions are analysed microscopically. The investigation is centred on a specific component with a load close to real application conditions but with varying load time. This creates an opportunity to investigate the degradation evolution under these particular conditions.

2. Samples and Testing

Investigated samples are primarily high power ($1700V/1000A$) IGBT modules with six sections running in parallel. On each section are two IGBTs/diodes and twenty $400\mu m$ heavy Al bond wires, see Fig. 1. Chips are soldered onto a standard Al_2O_3 DCB with a $100\mu m$ lead free solder paste. To separate individual module components sections are numbered from 1-6, LS and HS chips are separated, and wires are numbered from 1-10 inwards. In all cases numbering is from the section closest to the gate terminals and inward, see Fig. 1.

Regarded samples are stressed using an advanced

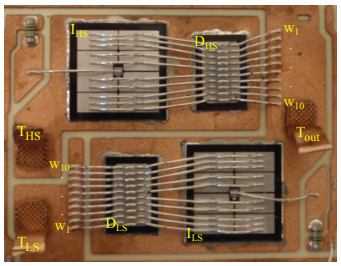


Figure 1: Image of single IGBT module section.

power/thermal cycling (A-TC) approach at accelerated conditions. The load profile is designed to stress the section diodes additionally, accordingly these are expected to fail initially. In order to avoid catastrophic events, like burnout, the majority of samples are removed from operation before failing through online monitoring. For details concerning the power cycling setup see [10, 8].

Five different samples are regarded, each subjected to a different number of samples, see Table 1. A_{New} is included to evaluate initial conditions and provide basis for comparison to stressed components. $F_{100\%}$ is introduced to create an estimate of present status in component lifetime.

Table 1: IGBT module samples. Abbreviations are identical to notation used in [11] for comparing data.

Name	**# cycles** [e6]
A_{New}	0
$C_{50\%}$	2.5
$D_{70\%}$	3.5
$E_{90\%}$	4.5
$F_{100\%}$	5.1

3. Methods

The characterization of device interconnect robustness and degradation evolution is centred on primarily two approaches: micro-sectioning and scanning electron microscopy (SEM) combined with focused ion beam milling (FIB). In the following a brief introduction is provided, for detailed information see [12, 13].

Presented thermal simulations are carried according to the procedure described in [14].

3.1. Micro-Sectioning

In Fig. 1 a layout of one of the module sections is presented. This is complex geometry with numerous of layers and sub-components. Characterization of a given region/interface is therefore complicated on many levels. With respect to investigation of failure mechanisms, samples of interest are in a damaged state. This renders it necessary to place considerable effort in maintaining a steady state after beginning a given investigation. The micro-sectioning approach is centred on: *(1) embedding the sample in epoxy for protection, (2) mechanical removal of unnecessary parts, (3) mechanical grinding until reaching desired interface, (4)* fine grade polishing, and *(5) electro-etching and optical microscopy*.

The electro-etching is included to promote grain structures in the Al wires. This is because the grain structure in the Al-wire/chip interface and its robustness is directly coupled[15, 16]. To promote the color contrast between grains after the etching the microscopy has to be conducted using polarized light[17, 18, 19, 20].

3.2. SEM/FIB Investigation

SEM is applied to obtain high resolution images of the metallization surface as well as the cross-sectional cuts obtained by micro-sectioning. Furthermore, by introducing FIB milling of the metallization cross-sectional views are obtained in very high resolution at any position on the surface. The equipment applied is a Zeiss 1540 XB SEM/FIB.

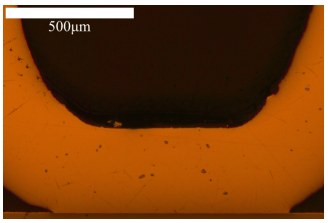
4. Results

4.1. Initial Observations

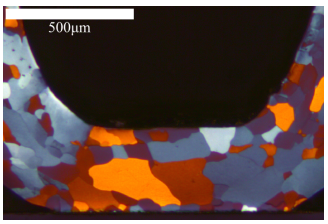
Using the approach described in Sec. 3 cross-sectional views of the wire bond interface may be obtained. In Figs. 2 three cross-sectional images of wire/chip interfaces are presented. Fig. 2a shows a stitch bond on top of a diode from A_{New}. On the right hand side the bond termination is close to ideal, whereas the left hand side displays a possible source of fracture initiation. Similar images are presented for a stitched bond on top of a diode (Fig. 2b) and an IGBT (Fig. 2c) but after electro-etching. The difference in wire curve after the stitch bonds are a clear source of unnecessary stress. After diode bonds the wire is observed to rise significantly steeper than at IGBT bonds. This has been shown to directly affect wire bond lifetime[21, 22].

4.2. Bond Wire Lift-Off

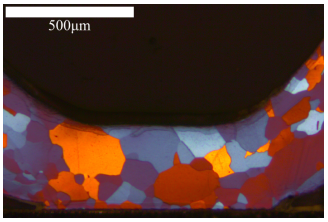
In Figs. 3, 4, and 5 cross-sectional views of an end bond interface on the LS IGBT is presented for samples $C_{50\%}$, $D_{70\%}$, and $E_{90\%}$, respectively. The motivation for choosing these particular bonds are the possibility to follow the fracture evolution. Degree of damage on LS diodes were to significant, see [11]. On the IGBTs the degree of bond degradation is observed to be proportional to number of cycles as would be expected. Furthermore, the wire propagation process seems to change with number of cycles as well. Initially, fractures tend to propagate between wire and metallization which is referred to as delamination. At later stages the crack moves intergranularly inside the wire itself combined with transgranular fracture across certain grains. Transganular propagation is not observed to depend directly on possible propagation paths, but more on grain type. In the insert in Fig. 4 a transgranular fracture is observed in spite of more ideal intergranular path. At a later stage a vertical intergranular path has been preferred instead of transgranular.



(a) Wire/chip interface on diode of A_{New}.



(b) Wire/chip interface on diode of A_{New} electro-etched.



(c) Wire/chip interface on IGBT of A_{New} electro-etched.

Figure 2: Wire/chip interfaces on top of diode (a)-(b) and IGBT (c) from a new power module (A_{New}).

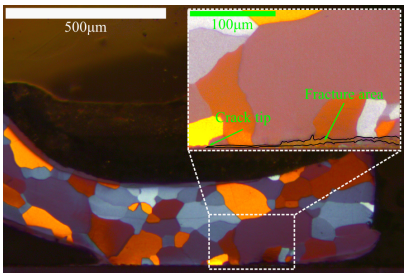


Figure 3: Wire/chip interface of end bond on IGBT from $C_{50\%}$. The insert illustrates the fractured area and the position of the crack tip.

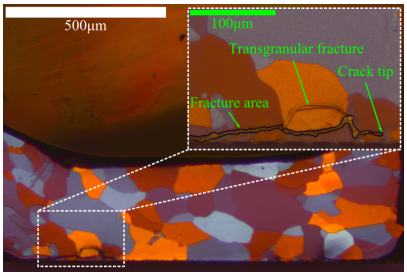


Figure 4: Wire/chip interface of end bond on IGBT from $D_{70\%}$. The insert illustrates the fractured area, position of the crack tip, and an transgranular fracture.

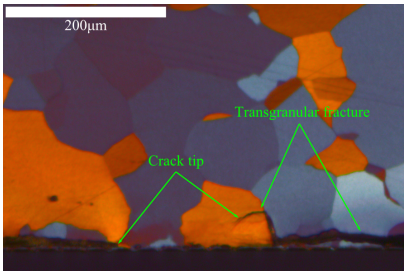


Figure 5: Wire/chip interface of end bond on IGBT from $E_{90\%}$. A large number of transgranular fractures are observed.

4.3. Metallization Reconstruction

As presented in Sec. 2 the A-TC load profile is designed to stress the module diodes. Therefore, no reconstruction effects are observed on the IGBT chips, see [11]. The diodes on the other hand are experiencing significantly reconstruction effects.

In Fig. 6 a topographic SEM image of the diode metallization from A_{New} is presented. A flat smooth polycrystalline surface is generally observed on all diodes from A_{New}, as would be expected.

In Figs. 7 topographic SEM images of diode met-

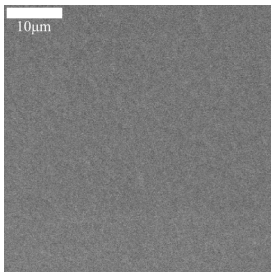


Figure 6: Diode metallization surface SEM images of A_{New} diode.

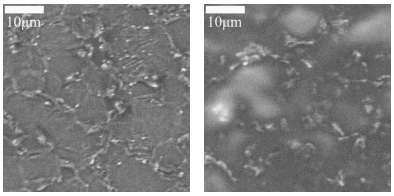
allizations from stressed devices are presented. (a), (c), and (e) are near the LS chip edge of $C_{50\%}$, $D_{70\%}$, and $E_{90\%}$, respectively. Similarly, (b), (d), and (f) are near the chip centres. A clear difference between different samples, and position on chip surface is observed with an increased degree of reconstruction. No apparent difference is observed between LS and HS devices.

Figs. 8 presents cross-sectional views of the metallization of LS diodes of $C_{50\%}$ and $E_{90\%}$. Cross-cuts are obtained by FIB milling. The reconstruction depth as well as extrusion effects are generally observed to increase with number of power cycles. Clear tendencies of cavity creation are observed in modules $D_{70\%}$ and $E_{90\%}$ near the diode centres.

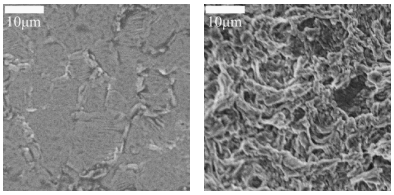
4.4. Thermal Simulations

In Fig. 9 the mean temperature (T_m) in 11 spots across the diode diagonal is plotted with the temperature variation (ΔT). The chip centre is clearly observed at the highest medium and peak value as would be expected. Furthermore, the ΔT is also observed to drop nearing the chip edge. On the LS IGBT the mean bond temperature of wires 1-5 range from $109.8 - 118.8°C$ and ΔT $24.5 - 31.7°C$ with no observed reconstruction.

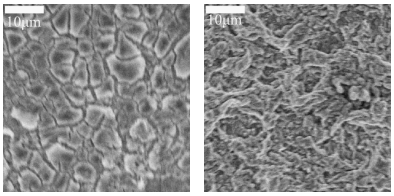
The plot is misleading with respect to mean junction



(a) $C_{50\%}$ LS diode edge. (b) $C_{50\%}$ LS diode centre.

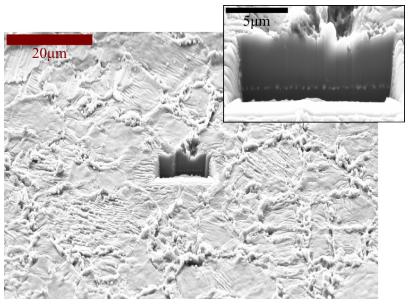


(c) $D_{70\%}$ LS diode edge. (d) $D_{70\%}$ LS diode centre.

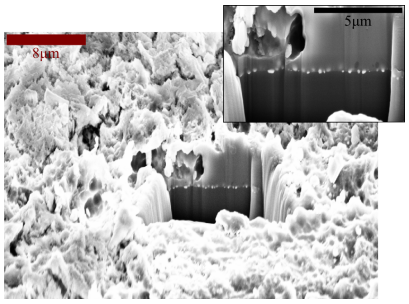


(e) $E_{90\%}$ LS diode edge. (f) $E_{90\%}$ LS diode centre.

Figure 7: Diode metallization surface SEM images of A-TC samples.



(a) $C_{50\%}$ LS diode centre.



(b) $E_{90\%}$ LS diode centre.

Figure 8: Diode metallization SEM/FIB cross-sectional images of A-TC samples.

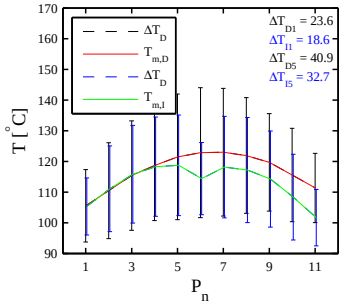


Figure 9: Mean temperature in 11 spots on chip surface across diagonal of LS diode and IGBT with ΔT around.

temperature because the IGBT chip volume is significantly larger. The gate region around P_6 displays a significantly lower temperature thereby lowering the mean junction temperature.

5. Discussion

5.1. Bond Wire Lift-Off

In Sec. 4.1 cross-sectional images of the power module wire bonds from a new sample are presented. From initial observations it is seen that stitch bonds tend to be more poorly terminated than end bonds, especially diode bonds due to the steep wire rise after the bond, see Fig. 2a. Compared to optimized samples, as discussed in [13], the *Al* grains are extremely large. This has a direct impact on the bond fatigue robustness through the Hall-Petch equation[15]. From micro-sectioning investigations it is apparent that the LS diodes are severely more damaged than the remaining components at an highly accelerated level, see [8]. Therefore investigation of the fracture process is primarily centred around the IGBT wire bonds.

The wire lift-off process is illustrated in Figs. 3, 4, and 5 of wire/chip interfaces of IGBT end bonds from samples $C_{50\%}$, $D_{70\%}$, and $E_{90\%}$, respectively. In all figures the wire lift-off process is observed as a hybrid of wire delamination and actual intergranular fracturing. In Fig. 3 a significant part of the wire bond is already fractured and the crack is seen to move close to the chip surface. But the fracture is primarily seen to move between grains or intergranular as would be expected. However, when regarding samples subjected to a higher number of cycles, see Fig. 4 and 5, the fracture path is seen to move within grains, or transgranular, as well. In both interfaces the bond degradation process is close to wire lift-off and especially $E_{90\%}$ displays many transgranular fractures.

All-in-all the wire fatigue observed in the samples are consistent with the wire bond quality in the new samples. The large grains makes the fracture propagate close to the chip surface, and not inside the wire itself as would be preferred. Furthermore, the grains are of so large a diameter that the fracturing tends to occur transgranular at later stages in lifetime. It is worth noting that no consistency between fracture direction options and transgranular propagation is observed. It is speculated that this could be connected with grain direction compared to fracture path, however, additional information from alternative methods is needed to verify this.

5.2. Metallization Reconstruction

In Figs. 7 the LS diode metallization surface is presented near the centre and edge of the chip for the three stressed devices. The difference between edge and centre images, as well as the degree of degradation being proportional to number of cycles, is consistent with metallization reconstruction being a thermal induced low-cycle fatigue process, see Fig. 9. The significant difference in temperature between edge and centre explains the difference in reconstruction. However, the limited difference in T_m and ΔT between IGBT and diode at the edge indicates a threshold induced phenomena highly dependent on ΔT. There is the possibility of coupling with current density, which are significantly lower near the edge of the IGBT.

In Fig. 8 FIB milling has been employed to create cross-sectional images of the metallization to investigate the vertical reconstruction effects. A clear increase of cavity depths are observed when increasing number of cycles or when comparing chip edges to centre. The reconstruction process appears solely thermally induced. No sign of electro-migration or severe diffusion processes are observed. However, this is not conclusive, additional tests without current loading are needed.

Near the end of the module lifetime the metallization is observed to be in a sheet like structure instead of a solid film. This could be a critical situation with either highly reduced film thickness or loss of contact to parts of the semiconductor.

6. Conclusion

This paper presents an investigation of degradation evolution and distribution of power module interconnects. The power module were subjected to active thermal cycling under sinusoidal loading with accelerated conditions (high medium temperature, low output frequency). Under these circumstances primarily wire bonds and chip metallizations were damaged. The former was identified in all connections of the regarded device, whereas the latter was only found on the component diodes.

Fracture propagation inside the wire interfaces of the IGBT *Al* bonds were observed to change from delamination between wire and substrate to intergranular fracture inside the wire to transgranular with an increasing number of power cycles. While increased damage is consistent with wire lift-off being a gradual degradation process the change of fracture phase without specific pattern is unexpected. One explanation of this could be connected with grain orientation with respect

to ideal fracture path. Additional information is, however, needed to verify this.

Metallization reconstruction was only observed on sample diodes indicating increased junction temperature. Furthermore, reconstruction was significantly increased near chip centre indicating hot spot effects as would be expected. While the mean chip temperature is significantly higher in the diodes compared to IGBTs[14], the surface temperature in specific spots are not necessarily higher in certain regions, see Fig. 9. Especially near the diode and IGBT corners identical mean temperatures are observed. This indicates that reconstruction effects are induced at a specific threshold between T_m and ΔT or the process couples with other mechanisms like current density. Accelerated tests under similar conditions but without applied currents would be a possible way to investigate this.

Acknowledgment

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References

[1] W. Kanert, Microelectronics Reliability 52 (2012) 2336–2341.
[2] M. Held, P. Jacob, G. Nicoletti, P. Scacco, M.-H. Poech, Power Electronics and Drive Systems (1997) 425–430.
[3] S. Ramminger, P. Trkes, G. Wachutka, Microelectronics Reliability 38 (1998) 1301–1305.
[4] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, M. Berkani, Industrial Electronics, IEEE Transactions on 58 (2011) 4931–4941.
[5] M. Ciappa, Microelectronics Reliability 42 (2002) 653–667.
[6] G. Z. Wang, Z. N. Cheng, K. Becker, J. Wilde, Journal of Electronic Packaging 123 (2001) 247–253.
[7] V. Smet, F. Forest, J. Huselstein, A. Rashed, F. Richardeau, Industrial Electronics, IEEE Transactions on 60 (2013) 2760–2770.
[8] P. Ghimire, K. B. Pedersen, B. Rannestad, A. R. de Vega, S. Munk-Nielsen, P. B. Thøgersen, Submitted to IEEE Transactions on Power Electronics (2014).
[9] R. Schmidt, U. Scheuermann, in: Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, pp. 1–9.
[10] A. R. de Vega, P. Ghimire, K. B. Pedersen, I. Trintis, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P. B. Thøgersen, in: Proceedings of the International Power Electronics Conference, pp. 2547–2553.
[11] K. B. Pedersen, L. H. Østergaard, P. Ghimire, V. Popok, K. Pedersen (2014). Submitted to: IEEE Transactions on Device and Materials Reliability.
[12] K. B. Pedersen, P. K. Kristensen, V. Popok, K. Pedersen, Microelectronics Reliability 53 (2013) 1422–1426.
[13] K. B. Pedersen, P. K. Kristensen, V. Popok, K. Pedersen, Journal of Materials Science: Materials in Electronics 25 (2014) 2863–2871.
[14] K. B. Pedersen, K. Pedersen, Submitted to IEEE Transactions on Power Electronics (2014).
[15] N. Hansen, Scripta Materialia 51 (2004) 801–806.
[16] W. Becker, S. Lampman, ASM Handbook Volume 11, Failure Analysis and Prevention (ASM International) (2002).
[17] G. F. V. Voort, ASM Handbook: Volume 9: Metallography And Microstructures, ASM International, 2004.
[18] E. Weidmann, A. Guesnier, Application notes - Metallographic preparation of aluminium and aluminium alloys, Technical Report, Struers A/S, 2008.
[19] M. Mohmmadtaheri, Metallography, Microstructure, and Analysis (2012).
[20] E. C. W. Perryman, J. M. Lack, Nature 167 (1951) 479.
[21] B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, M. Thoben, Microelectronics Reliability 52 (2012) 2353–2357.
[22] B. Czerny, I. Paul, G. Khatibi, M. Thoben, Microelectronics Reliability 53 (2013) 1558–1562.

IGBT MODULE RELIABILITY - PHYSICS-OF-FAILURE BASED CHARACTERIZATION AND MODELLING

PÅLIDELIGHED AF IGBT MODULER - PHYSICS-OF-FAILURE BASERET KARAKTERISERING OG MODELLERING

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This thesis has been submitted for assessment in partial fulfillment of the PhD degree. The thesis is based on the submitted or published scientific papers which are listed on the following page. Parts of the papers are used directly or indirectly in the extended summary of the thesis. As part of the assessment, co-author statements have been made available to the assessment committee and are also available at the Faculty. The thesis is not in its present form acceptable for open publication but only in limited and closed circulation as copyright may not be ensured.

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List of Papers

A **K. B. Pedersen, P. K. Kristensen, V. Popok and K. Pedersen**, *Microelectronics Reliability*, vol. 53, pp. 1422-1426, 2013.

B **K. B. Pedersen, P. K. Kristensen, V. Popok, and K. Pedersen**, *Journal of Materials Science: Materials in Electronics*, vol. 25, no. 7, pp. 2863-2871, July 2014.

C **K. B. Pedersen, P. K. Kristensen, V. Popok, and K. Pedersen**, *IEEE Transactions on Power Electronics*, 2014, in press - DOI: 10.1109/TPEL.2014.2344174.

D **P. Ghimire, K. B. Pedersen, A. R. de Vega, B. Rannestad, S. Munk-Nielsen, and P. B. Thøgersen**, *Proceedings of the 8th International Conference on Integrated Power Electronic Systems*, 2014, ISBN: 978-3-8007-3578-5.

E **P. Ghimire, K. B. Pedersen, B. Rannestad, A. R. de Vega, S. Munk-Nielsen, and P. B. Thøgersen**, "*Real time wear-out monitoring test setup for high power IGBT modules under sinusoidal loading condition*," Submitted to *IEEE Transactions on Power Electronics*, 2014.

F **K. B. Pedersen and K. Pedersen**, "*Dynamic modelling method of electro-thermo-mechanical degradation in IGBT modules*," Submitted to *IEEE Transactions on Power Electronics*, 2014.

G **K. B. Pedersen, L. H. Østergaard, P. Ghimire, V. Popok, and K. Pedersen**, "*Degradation mapping in high power IGBT modules using four-point probing*," Submitted to *Microelectronics Reliability*, 2014.

H **K. B. Pedersen, L. H. Østergaard, P. K. Kristensen, P. Ghimire, V. Popok, and K. Pedersen**, "*Degradation evolution in high power IGBT modules subjected to sinusoidal current load*," Finished - to be submitted, December 2014.

1* **K. B. Pedersen and K. Pedersen**, "*Bond wire lift-off in IGBT modules due to thermomechanical induced stress*," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems*, 2012, pp. 519-526.

2* **A. R. de Vega, P. Ghimire, K. B. Pedersen, I. Trintis, S. Beczckowski, S. Munk-Nielsen, B. Rannestad, and P. B. Thøgersen**, "*Test setup for accelerated test of high power IGBT modules with online monitoring of Vce and Vf voltage during converter operation*," in *Proceedings of the International Power Electronics Conference*, 2014, pp. 2547-2553.

3* **R. Wu, K. B. Pedersen, H. Wang and F. Blaabjerg**, "*Physics-based transient thermal impedance analysis of IGBT power modules under power loss/ambient temperature variation with experimental validation*," Finished - to be submitted, December 2014.

4* **P. Simesen, K. B. Pedersen, E. Skovsen, and K. Pedersen**, "*Grain structure mapping using second-harmonic generation (Working title)*," To be submitted, January 2015.

5* **P. Ghimire, K. B. Pedersen, P. K. Kristensen, and S. Munk-Nielsen**, "*Precise thermal imaging on high power IGBT module (Working title)*," Will be submitted to Bodo's Power Magazine, January 2015.

6* **K. B. Pedersen, P. Ghimire, P. K. Kristensen, S. Munk-Nielsen, and K. Pedersen**, "*High Resolution Simulation and Thermography of Temperature Fields in High Power IGBT Modules*," To be submitted, January 2015.

(*)Papers not included in the thesis.

List of Presentations

As a part of the Center of Reliable Power Electronics (CORPE) platform results and plans were presented on monthly basis at work package meetings, internal workshops, and group meetings. The following list only includes presentations outside these events.

1. Poster presentation AAU Materials Workshop, 2012
2. Oral presentation PEDG, June 2012
3. Poster presentation CORPE Annual Symposium #1, November 2012
4. Poster presentation ESREF, October 2013
5. Poster presentation CORPE Annual Symposium #2, November 2013
6. Oral presentation Fraunhofer IZM Power Electronics Group, January 2014
7. Oral presentation Danfoss Power Silicon Wissensforum, May 2014
8. Oral and poster presentation CORPE Annual Symposium #3, November 2014

Contents

Acronyms

IGBT	insulated gate bipolar transistor
BJT	bipolar junction transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
DCB	direct copper bonded
PWM	pulse width modulation
DUT	device under test
CTRL	control side
HS	high side
LS	low side
DC	direct current
AC	alternating current
A-TC	active thermal cycling
P-TC	passive thermal cycling
CTE	coefficient of thermal expansion
SEM	scanning electron microscopy
EBSD	electron backscattered diffraction
FIB	focused ion beam
US	ultrasonically wedge
FEM	finite element method
BC	boundary condition
PID	proportional-integral-derivative
EMA	effective medium approximation
EDX	energy dispersive X-ray spectroscopy
CAD	computer aided design

List of Figures

List of Tables

Preface

In the three years it has taken to complete the work presented in the thesis many people have contributed to improve the scientific quality and the process itself. This support has been vital in order to fulfil the presented work.

Initially, I would like to thank Kjeld Pedersen for guidance, support, and the opportunity to work on the presented topics. Especially, the freedom to follow new ideas and opportunities along the way has been essential during the last three years. Additionally, I would like to thank Peter Kjær Kristensen for significant assistance with experimental work and discussions on numerous topics. I would like to thank Vladimir Popok for his general contributions which has improved the overall level of the work. Furthermore, thanks to Pramod Ghimire for the opportunity to collaborate on interesting topics in the world of testing power modules. I would like to thank Eckart Hoene for the opportunity to visit Fraunhofer IZM, Berlin for three months and participate in ongoing projects. The insight into relevant topics and the work process of other groups is always interesting.

I would like to thank the office gang - Mads Lund Trolle and Søren Vejling Andersen for the good times we have had sharing an office. The countless pure expert discussions we have had, are very appreciated!

Finally, I would like to thank my friends and family for their understanding and support when work has been put in front of everyday events. A special thanks to my girlfriend Maria who with her patience and never-ending support has been amazing!

Part I

Introduction

Reliability of Power Electronics

Power devices are today found in a large range of applications, from consumer electronics (battery chargers, mobile phones, etc.) to high power electronics (traction, automotive, electrical power transmission/distribution, etc.)[1, 2]. Accordingly, the load experienced by a component varies significantly. The voltage may vary from a few volts to several kilo volts and similarly with respect to currents. Furthermore, surrounding environment may vary from the inside of a mobile phone to an off-shore wind turbine. Under these stringent circumstances the device is expected to perform within product specifications in a reliable way. Reliability of a system is defined as the ability to perform its function under given conditions for a required amount of time[3, 4]. In power electronic systems and especially for high power modules the expected useful lifetime is rarely below 10 years and often around 30 years.[2, 5]

In the present work focus is placed on power electronics applied in energy conversion - specifically power modules. This is an extremely significant area as electrical energy today constitutes more than 40% of the total global energy consumption. This percentage is increasing every year due to interests in alternatives to fossil fuels[6]. By 2020 members of the EU have agreed to increase the percentage of renewable energy and reduce CO_2 emissions by 20%[7]. Based on this the interest in reliable and efficient components is significant due to economical as well as safety reasons. An example of the former could be the spontaneous failure of an off-shore wind turbine, whereas the latter could be failing of safety equipment during the accident[1].

A direct approach ensuring reliable device performance would be to apply component testing under the required conditions until failure for numerous samples. This, however, is not convenient as the expected lifetime could be in the range of 30 years. A solution to this has been to conduct tests under accelerated conditions and combining data with model fitting and extrapolation to normal operation conditions[8, 9]. By establishing a method of predicting the lifetime of the component in question, one could take preventative actions prior to failure. The problem with such predictions is the extrapolation of data from limited periods of accelerated testing to a 10-30 year lifetime, as well as inaccuracy of the applied model[10, 11]. Several attempts of constructing applicable models for such lifetime estimation methods has been done, varying from more or less advanced statistical models [8, 12–14] to more physics-of-failure related approaches [15–17]. While the former requires a large number of sample tests at various conditions to ensure a high degree of statistical certainty, the latter needs detailed knowledge regarding the component's physical properties as well as degradation evolution.

In the present work the situation of high power insulated gate bipolar transistor (IGBT) modules subjected to power cycling or active thermal cycling (A-TC) is regarded. Typical A-TC tests are performed by applying a constant direct current (DC) pulse for a given time

followed by a cool down[1, 5, 12][*1]. The power loss from the applied current heats up the system thereby inducing thermal stress in the component. Depending on the on-time versus off-time the number of elements inside the power module affected by the heating is changed. At the same time the effect from applied load depends highly on the surroundings, if A-TC tests are performed at $100^{\circ}C$ compared to $20^{\circ}C$ the module power loss, module thermal properties, and individual material properties are highly affected. Therefore, by changing the load amplitude, load time, and surrounding environment the test in principle changes[18]. With short pulses ($< 5s$) and stress close to real world application $\Delta T < 110K$ the dominating failure mechanisms observed in IGBT modules are thermo-mechanical degradation of interconnects[2, 8, 11, 19].

Thus, the overall scope of the presented work is investigation of degradation in high power IGBT modules subjected to conditions resembling real life. A combination of accelerated tests of present-day used power modules, microscopical characterization of material state and failure mechanisms, and 3D dynamical modelling of stressors and degradation gives an insight creating possibilities for component optimization, quality investigation, and lifetime estimation not requiring hundreds of end-of-life tests.

[*1] DC pulsed accelerated testing is not the used method in the present work, but for now we regard the concept to single out the relevant degradation mechanisms.

Thesis Summary

Overall the goal of the work behind the thesis is to increase the level of understanding of thermo-mechanical related failure mechanisms in high power IGBT modules by utilizing physics-of-failure based concepts in module design, fabrication, and application. Based on this the thesis is separated into three parts: (I) Introduction, (II) Test Setup and Characterization Techniques, and (III) Degradation Modelling.

In part I the basic concepts behind power module design/fabrication, failure mechanisms, and lifetime estimation are introduced. Standard fabrication approaches used on regarded devices are presented together with a brief overview of alternatives. Afterwards, the commonly experienced degradation and failure mechanisms are presented with a special focus on thermo-mechanical load. Finally, the normally applied test and lifetime assessment methods are discussed.

Part II introduces the majority of experimental work carried out. Initially, the accelerated test setups used to stress devices as well as their relevance are presented. An alternative method of doing active power cycling is introduced with closer resemblance to real life application compared to standard DC pulse tests. Together with the accelerated test setup a new methodology for utilizing online monitoring of electrical parameters are introduced which is able to separate degradation of individual module interconnects. In order to validate the online monitoring results, as well as map the degradation distribution, a four-point probing approach is developed for measuring the local degradation across specific interfaces. The method is applied on several different power modules subjected to a varying number of power cycles and compared to online monitoring results as well as micro-investigation. Finally, a micro-sectioning approach is presented for microscopy based investigation of failure mechanisms. The approach is centred on multiple techniques: mechanical steps for module separation, electro-chemical etching for grain structure analyses, and scanning electron microscopy/focused ion beam milling for micro analysis. The concept is utilized to: conduct detailed investigation of the ultrasonic wedge bonding process and possible ways of optimization, robustness evaluation, and characterization of failure mechanisms. Discussed results are presented in papers A, B, C, D, E, G, H.

In part III a dynamic 3D degradation model of thermo-mechanical related failures is presented. The model is based on a series of steps: power loss, temperature field, strain field, material degradation which are interconnected dynamically. Fundamental theory as well as motivation for model structure is introduced and discussed together with alternative approaches. The degradation model is used on the same system regarded in part II making it possible to directly compare results and evaluate model consistency. Model theory as well as results are presented in paper F.

Dansk Resume

Generelt er formålet med afhandlingen at hæve forståelsesniveauet omkring termomekanisk relaterede fejlmekanismer i højeffekt IGBT baserede moduler. Dette er for at kunne udnytte fysiske koncepter i modul design, fabrikation og anvendelse. Baseret herpå er afhandlingen inddelt i tre dele: (I) Introduktion, (II) Test Setup og Karakteriserings Teknikker, og (III) Nedbrydnings Modellering.

I del I omtales de grundliggende koncepter bag effektmodul design/fabrikation, fejlmekanismer og levetids estimering. Standard fabrikations metoder anvendt på de betragtede komponenter bliver præsenteret sammen med en kort oversigt over mulige alternativer. Efterfølgende præsenteres de normalt observerede nedbrydnings- og fejlmekanismer, med et specielt fokus på termomekanisk belastning. Endelig diskuteres de almindeligt anvendte test metoder samt modeller til levetids estimering.

Del II introducerer den primære andel af eksperimentelt udført arbejde. Indledningsvis præsenteres de accelererede test setups anvendt til at stresse de betragtede komponenter samt de pågældende metoders relevans. En alternativ test metode bliver foreslået som er tættere på almindelig applikation sammenlignet med DC puls tests. Sammen med den nye test metode introduceres en ny online overvågnings metode af elektriske parametre som kan anvendes til at separere nedbrydning af forskellige modul forbindelser. For at validere disse resultater samt at kortlægge nedbrydnings fordelingen udvikles et fire punkts probe setup til at måle den lokale nedbrydning henover udvalgte grænseflader. Metoden anvendes på adskillige forskellige effektmoduler der er blevet underlagt et forskelligt antal power cycles og sammenlignes med de førnævnte online monitored resultater samt mikro-analyse. Endelig præsenteres en mikro-analyse metode baseret på mikroskopi undersøgelse af fejlmekanismer. Metoden er centreret omkring flere teknikker: mekanisk separering af modul elementer, elektro-kemisk ætsning for undersøgelse af kornstrukturer, og skannende elektron mikroskopi kombineret med fokuseret ion stråle tværsnitsanalyse. Konceptet anvendes til at: udføre detaljeret analyse af ultrasonisk wedge bonding, muligheder for at optimere robusthed samt undersøgelse af fejlmekanismer. Resultaterne er primært introduceret i følgende artikler: A, B, C, D, E, G, H.

I del III præsenteres en 3D dynamisk metode til at modellere termomekanisk relateret fejlmekanismer. Modellen er baseret på en serie af skridt: effekttab, temperatur felter, belastning, og materiale nedbrydning. Disse er alle forbundet dynamisk. Fundamental teori samt motivationen bag model strukturen bliver introduceret og diskuteret sammen med alternative metoder. Nedbrydningsmodellen anvendes på det samme system som betragtes i del II, hvilket muliggør direkte sammenligning af resultater og derved overensstemmelse. Teori og resultater præsenteres primært i artikel F.

CHAPTER 1

Power Modules

The main purpose of high power modules are, as the name implies, to handle power. Regardless of design and application, three main properties are essential: current handling, blocking voltage, and power dissipation[5, Ch.11]. In general the semiconductor chips are the central components as the only active elements. In order to achieve optimal performance of semiconductor chips the device interconnections, housing, cooling reservoir, etc. has to fulfil a minimum of similar specifications.[20]

Today, in high power electronics IGBT chips are the most commonly used component due to the high blocking and current handling capabilities. IGBTs combine the current densities of the bipolar junction transistor (BJT) with the gate handling capabilities of the ordinary metal-oxide-semiconductor field-effect transistor (MOSFET). This creates a component able for high voltages, -currents, and -switching frequencies, which makes it ideal for high power applications e.g. in the automotive industry or in energy production[2, 21].

Utilizing advanced semiconductor chip designs, like the MOSFET and IGBT, has enabled the concept of housing several active components in the same module. If acting in parallel the current handling capabilities may be increased accordingly. This further increase the requirements of the module packaging. As before mentioned, the main purpose of the packaging is to provide a stable controlled environment, meaning mechanical stability, good thermal conductivity, and electrical insulation. Today, this is centred around three primary elements: module baseplate, packaging housing, and a direct copper bonded (DCB) substrates[2, 8, 20]. To simplify the fabrication the high current capabilities generated from multiple chips is obtained by introducing a section design concept with multiple identical sections.

1.1 IGBT Modules

In Fig. 1.1 an image of an actual IGBT module is presented. The precise module type is introduced later, for now we regard the layout. Six identical sections are placed in parallel on a baseplate. Each section is comprised of a DCB with two IGBT chips and corresponding free-wheeling diodes placed on top. The DCB based section design are by far the most commonly used[4, 22].

Connection between chips and the DCB is on one side obtained through a compliant solder and on the other side through standard heavy *Al* bond wires. All DCBs are attached to

the baseplate using the same solder paste. The image displayed in Fig. 1.1 is obtained after removing a plastic housing, a silicone gel covering all active elements, and the *Cu* terminals providing connection between the individual sections and the surrounding system.

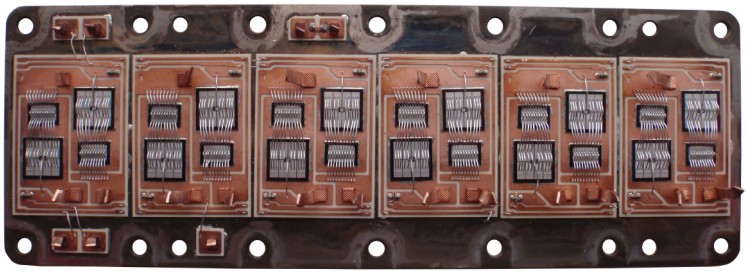
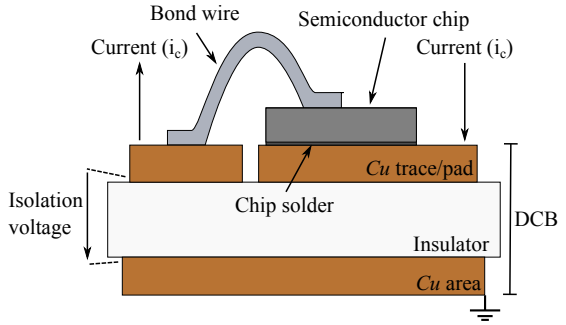


Figure 1.1: Image of IGBT power module without housing, silicone gel, and terminals.

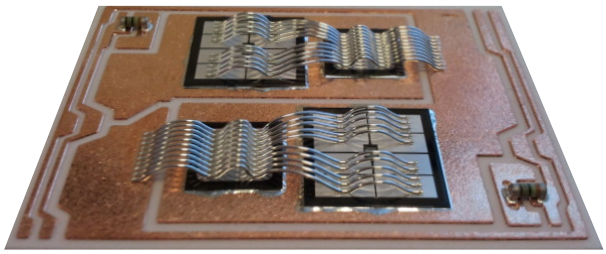
The design is common in modern power modules with the position and type of chips and interconnections depending on application. Silicone gel and plastic housing are added primarily for environmental protection (humidity, mechanical shocks, etc.). DCBs are used to provide electrical isolation, mechanical stability, and good thermal conductivity to the baseplate[5, 8, 20].

1.1.1 Section Design

In general materials in the IGBT module are chosen for their electrical properties, but just as importantly for their thermal properties. For example a common requirement is that the overall storage and operating temperatures should be between $-55°C$ and $175°C$[19]. Accordingly, plastics, metals, ceramics, silicone gels, etc. must be operational in this range. An illustration of an ordinary power module section design is depicted in Fig. 1.2:



(a) Illustration of a IGBT module cross-section, based on [4, 20].



(b) IGBT module section image, from paper B.

Figure 1.2: Cross-sectional view 1.2(a) and image 1.2(b) of IGBT module section.

The cross-sectional view only includes the layers from the DCB and upwards. Therefore, below the bottom *Cu* region of the DCB and additional solder layer is in the full power module attaching the section to the baseplate. On top of the DCB the semiconductor chips are attached to the *Cu* pad with a solder paste on one side and bond wires on the other. Finally, the entire module is encapsulated in silicone gel for protection against environmental effects and act as a secondary cooling path.

DCB Substrate

DCB substrates are comprised of a ceramic dielectric insulator with pure *Cu* applied and bonded on both sides, see Fig. 1.3 for a schematic. This process yields a great adhesive strength through a high temperature melting and diffusion process[20].

The main ceramics used in DCB substrates are aluminium oxide (Al_2O_3) and aluminium nitride (AlN)[*1]. These particular ceramics are chosen due to their high thermal conductivity compared to other insulators. While AlN has a significantly higher thermal conductivity, see Table 1.1, the coefficient of thermal expansion (CTE) is lower thereby increasing the

[*1] BeO ceramics was priorly, due to its very high thermal conductivity ($250 W m^{-1} K^{-1}$), used but was taken out of service due to the toxicity of BeO dust.[5]

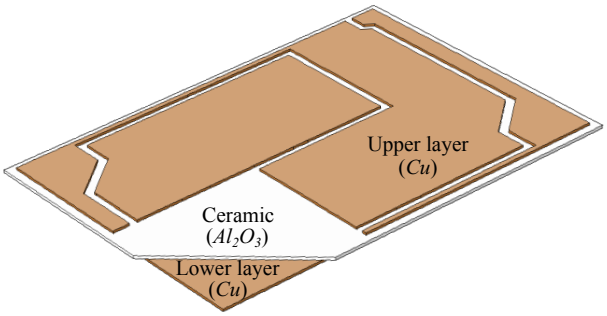


Figure 1.3: Illustration of DCB substrate.[20]

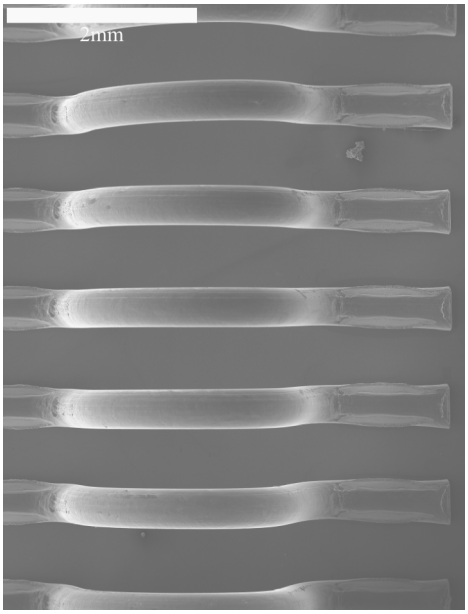
mismatch created stress to *Cu*. Futhermore, fabrication of substrates with *AlN* are more expensive due to additional steps in the bonding procedure. Based on this DCBs are chosen primarily by balancing need of conductivity versus cost.[5]

Bond Wires

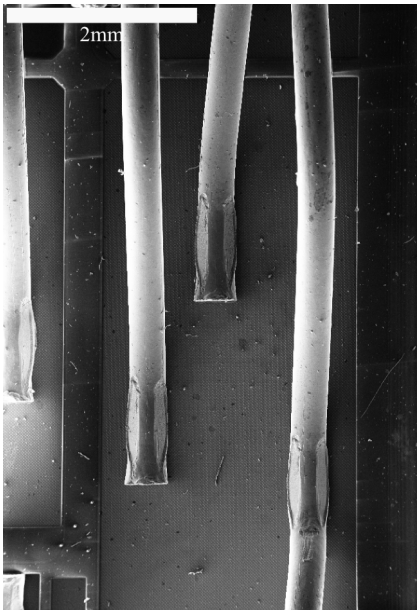
Bond wire interconnects have for many years been a preferred component in the design of *Si* based power modules on the chip emitter side. The most commonly used assembling technology has due to speed and quality been ultrasonically wedge (US) bonded 99.99% *Al* wires. In some cases small amounts of either *Si*, *Mg*, or *Ni* have been added to the wire for corrosion control or wire hardness.[23–27]

The bonding process and optimization of bond quality is discussed in detail in paper B. But in general the US bonding method is a solid state process carried out at room temperature with limited heating during bonding[28, 29]. The bonding itself is carried out in a number of steps (1)-(4) which create a strong polycrystalline interface, see Figs. 1.4 for topographic views.[28–32]

1. Wire hardening by applying a force through the wedge.
2. Reducing the yield and tensile strength of the Al wire by ultrasonic vibrations. A process normally called ultrasonic softening.
3. Deformation of the wire created by the two previous processes which enables diffusion and removal of impurities. The diffusion mentioned here is typically observed if the wire is not pure Al.
4. Ultrasonic hardening of the wire following the softening.



(a) SEM image of *Al* bond wires on top of diode.



(b) SEM image of *Al* bond wires on top of IGBT.

Figure 1.4: Topographic view of bond wires on top of (a) diode and (b) IGBT chip. Clear markings from the wedge bond tool are observed.

1.1.2 Baseplate

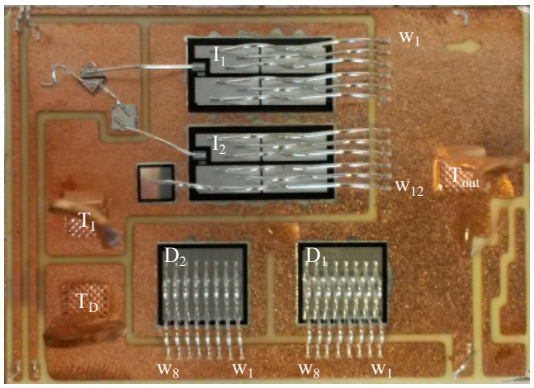
The commonly used baseplate material in high power modules is *Cu*. Main motivation for using this is the high thermal conductivity and the mechanical compliance with the bottom *Cu* layer of the DCB. Several alternatives to *Cu* baseplates exist, with the primary ones being *AlSiC* or no baseplate. The latter is a field in itself and is not a part of the present work. *AlSiC* is a metal matrix composite material manufactured by forming a porous *SiC* matrix and filling the pores with *Al*. Accordingly, the physical parameters depend on ratio between *Al* and *SiC* but generally *AlSiC* is a lightweight material with high stiffness[5, 33]. The majority of presently regarded samples are with *Cu* baseplates.

1.2 IGBT Module Samples

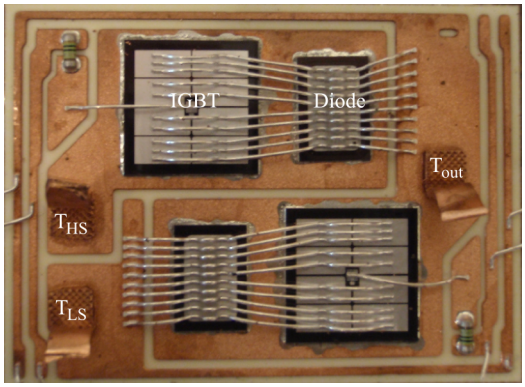
A number of high power IGBT module/section samples are regarded in the present work. All are present-day used components available in the market and will probably be so in several years, except for the ones presented in paper B. Here a test sample is fabricated for the sole purpose of investigating and optimizing the bonding process. In Figs. 1.5(a) and 1.5(b) two

module sections are presented. Both consist of two IGBT and diode chips connected to the DCB with *Al* bond wires. The section in Fig. 1.5(a) is chopper based design and the one in Fig. 1.5(b) is a halfbridge design.

Layer thickness and composition of the samples are presented in Table 1.1. Possible al-



(a) IGBT module section - chopper design.



(b) IGBT module section - halfbridge design.

Figure 1.5: Images of regarded IGBT module sections.

ternatives to baseplate and DCB ceramic is listed as well with typical thickness'. To illustrate the source of thermal stress the expansion coefficient α is listed for all layers.

Table 1.1: IGBT module layer thickness/composition and physical parameters at room temperature. All parameters are highly material dependent, accordingly, alloy composition is essential with respect to actual values.[2, 34]

Layer	**Material**	**d** $[\mu m]$	**k** $[W/(m \cdot K)]$	$\boldsymbol{\alpha}$ $[10^{-6}/K]$
Bond wire	Al	300-500	238	23
Metallization	Al	4-6	238	23
Chips	IGBT/diode - Si	200-300	130	2.6
Solder	$SnAg$ (96.5/3.5)	50-150	53.5	28
DCB	Cu	300	400	17
	Al_2O_3 or AlN	380 / 700	25 / 150	8.2 / 4.5
	Cu	300	400	17
Solder	$SnAg$ (96.5/3.5)	50-150	53.5	28
Baseplate	Cu or $AlSiC$	3000	400 / 190	17 / 4.7

CHAPTER 2

Failure Mechanisms and Lifetime

Numerous stressors may cause an eventual failure in a power module, a final catastrophic event is often a combination of many different processes[2]. One example of this is thermo-mechanical induced stress in interconnections which initially may cause local failures like lifting of a single wire which afterwards are followed by avalanche effects by the increased stress on the remaining wires. Finally, the failing of several connections may cause a device burn-out or explosion. In the present chapter we will centre the attention on thermo-mechanical induced failures in package interconnections and limit ourselves to a few mechanisms which may affect the overall device performance together with interconnection failures. [2, 4, 19, 35]

2.1 Selected Mechanisms

As mentioned, several mechanisms other than thermo-mechanical related may cause an eventual device failure, electromigration[36], cosmic rays[37], dielectric breakdown[38], etc. Here, only the topics relevant for the presently regarded modules subjected to specific conditions are presented.

2.1.1 Electromigration

With the ever decreasing scale of electronic components the concept of electromigration also becomes more relevant. Electromigration is the transport of mass created by pure momentum transfer between the electron current and host atoms. In order for this to occur at a critical scale a certain current density is necessary[36]. The process is especially critical in regions with current flux divergence, this diversity may be caused by micro-structural changes, temperature, local stress, or impurities. Mass migration can either create voids or cluster regions with the possibility of either increased resistance or open circuit conditions. For both *Al* and *Cu* based connections the dominant diffusion path of material is along grain boundaries. However, in the power modules considered presently the current densities should not be on the scale triggering significant electromigration effects from the beginning[*1]. But as will be discussed in a following section, thermo-mechanical induced material degradation could cre-

[*1] For *Al* $J^e_{crit} = 2e5A/cm^2$, for *Cu* $J^e_{crit} = 1e6A/cm^2$.[39]

ate narrow regions with possibility of migration issues. For additional information regarding the electromigration concept or modelling of failure time under a given condition see [38].

2.1.2 Corrosion

Corrosion in electronic materials are in principle identical to passive corrosion elsewhere, except for the applied voltage. So similar to other situations the main corrosion factors are temperature, relative humidity, fabrication contamination, and corrosive gasses. Generally, when having layered structures with *Al* the possibility of galvanic corrosion is present both under operation and fabrication. Other corrosive processes are possible as well depending on materials present and foreign elements (gasses, liquids). In all cases the outcome is normally an unacceptable increase in resistance or open circuit conditions. To rule out external impact the custom method is to protect the electronics using a plastic housing and a polymer. Moisture will still diffuse through but condensation on the device surface is not possible as long as the polymer adheres.[40]

2.1.3 Burnout Failures

Device burnout is often observed as a final act in a complete failure or as a consequence induced by another mechanism - e.g. wire lift-off. The mechanism is normally related to a short circuit situation where a high current is flowing through the device in selected regions. Supporting the short circuit situation for a long time period results in thermal runaway and thereby device destruction. In the short time frame of the process the regions are heated almost adiabatically which in the end cause catastrophic failure of the component.[2, 35]

2.2 Thermo-Mechanical Stress

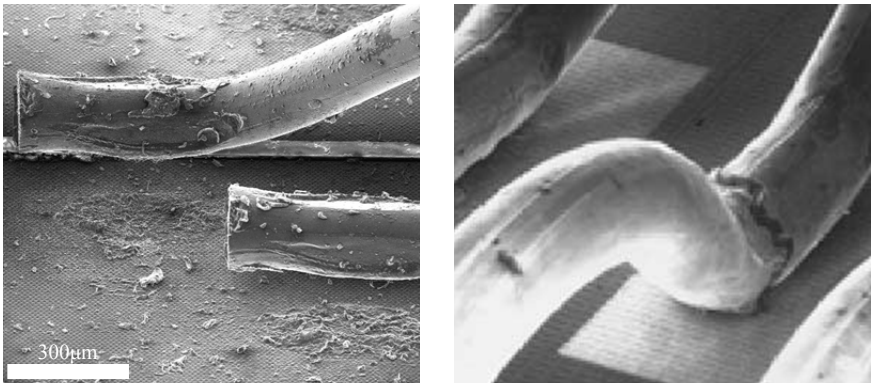
The standard application of power modules, as discussed later on, often involves highly fluctuating loads, both with regards to environmental and electrical loading. Both types create oscillations in the temperature inside the power module. The cyclic conditions, passive or active, cause a thermo-mechanical loading due to material expansion and CTE mismatch, see Table 1.1. Both of these directly affect the module packaging and especially the interconnects: solder joints, bond wires, metallization. Especially solder joints and bond wires have been known for years to be stressed by temperature changes.[25, 41]

2.2.1 Bond Wire Fatigue

Bond wire fatigue is a failure type in principle containing any thermo-mechanically induced failures related to the bond wires or wire bonds. It has often been divided into heel cracking[42] and lift-off[19] as the primary mechanisms, see Figs. 2.1. But in principle additional groupings could be created. In common, however, is that the primary stress is

induced by wire flexure and CTE mismatch[2, 22, 25].

The failure is the primary observed mechanism under low/medium stress conditions



(a) Bond wire lift-off. (b) Bond wire heel crack.

Figure 2.1: SEM images of bond wire fatigue failures, (a) lift-off and (b) heel crack. (a) is a lifted wire on the sample illustrated in Fig. 1.5(a) subjected to pulsed cycling. (b) is obtained from [2].

which is why it is often observed in power cycling[19]. Highest stress is normally observed near the wire terminations where the wire is unable to flex and the local stress cause a high strain, which in the end will initiate fractures. This process is discussed in detail in a later section. Both failures creates a basis for a domino effect after the first wire fails. The initial wire creates a non-homogeneous current distribution causing additional wear on surrounding elements. Due to the limited number of wires this type of degradation is often observed to cause a change in on-state voltage[7, 8]. In the final stages of the lift-off process a discharge is often observed to cause severe damage in the metallization surface, as seen in Fig. 2.1(a).[5]

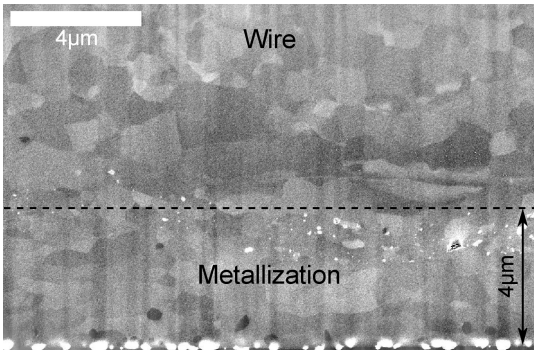
Normally, a significant amount of wire residue is observed on top of the metallization after a wire lift-off. This indicate the crack propagation path has been inside the wire itself[29, 43]. The reason for this is linked with the microscopical grain structure of the *Al* wire illustrating the necessity for a well-optimized bond. Bond optimization is not only a matter of changing US bonding parameters, see paper B, but also an ideal wire curvature[44, 45].

To prevent bond wire related failures several strategies have been and are being investigated. Ranging from solutions like strain buffers through an intermediate layer [27], different assembly methods like press pack designs and integrated systems[46], to *Al* wire alternatives like *Cu* wires[47, 48]. However, the alternatives are still not on a level where heavy *Al* bond wires are replaced in high power IGBT modules. This is primary due the design freedom the bond wires create, the low price, and the rather simple assembly procedure.

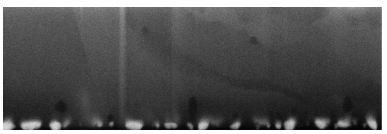
2.2.2 Metallization Reconstruction

In Sec. 1 the common design of a high power IGBT module was presented. To obtain direct electrical connection to all conducting channels of the semiconductor chips a metallization layer is added. The standard fabrication technique is adding a film of *Al* through physical vapour deposition combined with thermal annealing creating a polycrystalline structure with a grain diameter below $1\mu m$, see Figs. 2.2.[5, 400-403]

Similar to the stress on the bond wires, apart from the wire flex contribution, the CTE mismatch between *Al* and *Si* creates a high degree of stress in the interface when subjected to temperature oscillations. In Table 1.1 α is presented for *Al* and *Si* indicating that during warm-up the metallization suffers from compressive stress and vice versa for the chip. However, only elastic strain is normally observed in the chips due to the high yield strength of *Si*. *Al* relaxation does not occur directly in the interface, even though the stress is highest here, due to compression on both sides. Instead metallization surface effects are observed through grain extrusion or general reconstruction[19], see Figs. 2.3. This cause an increase in the effective sheet resistance[49] and in some cases cause critical regions with high current densities and thereby possibility of electro-migration[8]. Similar to wire bond degradation, reconstruction is a continuous process with a degradation rate proportional to absolute loading and pattern, which in the end may cause avalanche effects.[19]

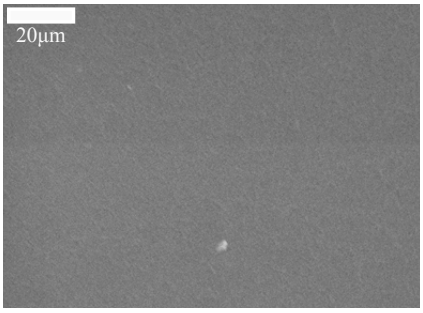


(a) SEM/FIB image of metallization underneath wire bond.

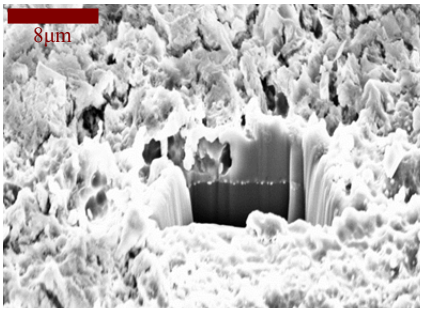


(b) SEM/FIB image of metallization at edge of wire bond press area.

Figure 2.2: SEM/FIB images of metallization micro-structure - both figures are from paper B.



(a) SEM image of metallization surface.



(b) SEM/FIB image of reconstructred metallization.

Figure 2.3: SEM/FIB images of metallization - (a) illustrate a new metallization and (b) a severely reconstructed. Both images are of the type illustrated in Fig. 1.5(b).

2.2.3 Solder Fatigue

In the geometry presented in Fig. 1.1 a solder layer is connecting both the chips to the DCB and the sections to the baseplate. Fatigue are experienced in both layers but with different loads[9, 50]. The primary stress is still temperature induced, due to CTE mismatch, which is the cause of the difference. Positioned directly underneath the chip this solder layer is heated rapidly in the same way as the wire bonds and the metallization, whereas the baseplate attachment layer is experiencing a delay. The solder composition depends on application - temperature range, regulations, etc. But the common composition is as listed in Table 1.1.

The main impact from bad solders (fractures, voids, delamination) is thermal[51]. During operation the solder provides the primary thermal path away from the chip meaning that a reduced connected area directly affects the chip temperature. This can be edge effects like illustrated in Fig. 2.4 but also in the centre of the solder due to voids from production. The effect from the raised temperature depends on the application level, if the chip loading is in a region with a negative temperature coefficient on the forward voltage the effective power loss is not directly increased. However, the surrounding elements (metallization, wire bonds, etc.) are often stressed additionally because the temperature distribution is often changed[9]. The degradation process is still progressive and irreversible as with reconstruction and wire fatigue. Main difference is the irreversible processes. The solder structure makes the degradation process more viscoplastic and thereby highly time and rate dependent (creep).[52]

2.3 Power Module Test Methods

Overall, the main purpose of testing components is to ensure robustness and reliability with respect to a given application. Numerous factors affect power module reliability: electrical

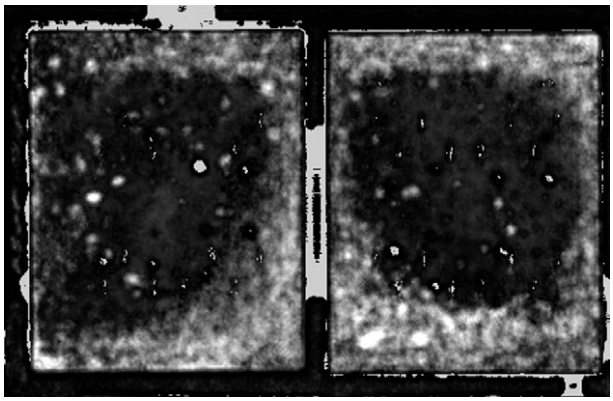


Figure 2.4: Chip solder delamination obtained using a ultrasonic scan - image is from [9].

load, environmental (temperature, humidity), mechanical (vibrations, shocks), etc. Accordingly, a full real life simulation is not possible to perform in a test setup. Based on this the main outset in test setup design has been to introduce the most severe fundamental conditions. For power module packaging this has been centred around two methods: active power cycling/A-TC and passive thermal cycling (P-TC).[8, 53]

Based on application purpose a setup emulating normal operating conditions are not necessarily optimal for robustness or end-of-life evaluation. In numerous application areas the expected component lifetime exceed 10 years, accordingly, end-of-life tests should ideally require the same time. A solution to this problematic has been to employ accelerated conditions through increased stress levels. This, however, present other problems. One example of this is observed in thermo-mechanical related failure mechanisms. Here the general test approach has been to control the mean temperature (T_m) and induce a specific temperature variation (ΔT). However, by increasing ΔT above normal operation conditions one risk inducing material related mechanisms normally not observed.

P-TC is normally conducted by heating the entire device up and down by moving it physically between a heated and cooled chamber, see Fig. 2.5(a). The time required in each chamber is often relatively high to ensure the entire device reaches the desired temperature. One of the main purposes of the test is to conduct thermo-mechanical robustness tests on the entire geometry and not only elements heating during active operation.

A-TC is normally created through on-state losses from an alternating current (AC) or a pulsed DC. In later years the latter has been the dominant approach for IGBT and MOSFET based modules, see Fig. 2.5(b). One reason for this is the possibility to estimate average chip junction temperature through on-state voltage at the end of each pulse. This makes it possible to online monitor the changes during power cycling. This will be discussed in detail in a following section. The main advantage of A-TC compared to P-TC is the closer resemblance to real-life operation where the thermal load is generated around the chips. Mainly two measuring schemes are being used: *(1)* constant junction temperature variation (ΔT)[54], *(2)*

constant pulse times (t_{on}/t_{off})[55]. The difference lies in the methods response to device degradation. Under constant ΔT the pulse width needs to be varied in order to accommodate constant loading. This means that if on-state voltage increases due to e.g. bond wire lift-off the on-state time needs to be decreased an vice versa with lower forward voltage. The second scheme on the other hand maintains constant pulse time until a given criteria, meaning the ΔT is allowed to vary.[12]

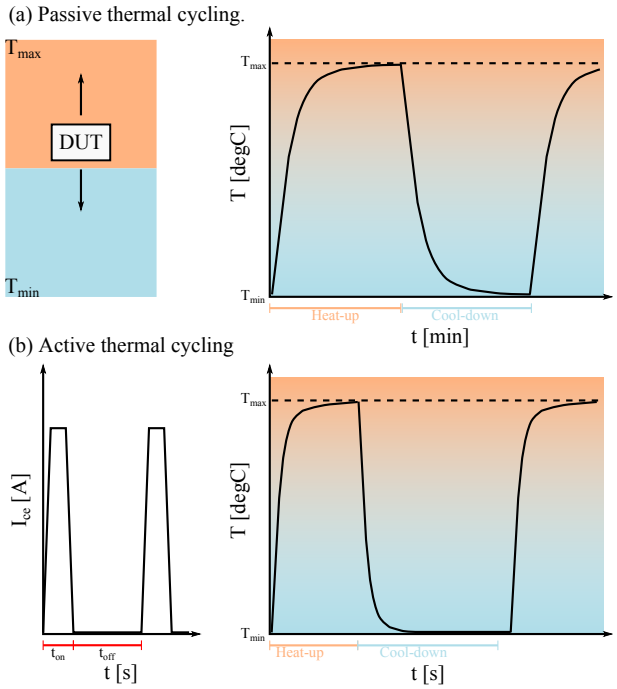


Figure 2.5: Illustration of power cycling approaches (a) P-TC and (b) A-TC - inspired from [18].

2.4 Lifetime Estimation

As presented in Cha. 2 there are several different mechanisms creating damage in high power IGBT modules and for each one a different lifetime estimation method exist. The present section is limited to models trying to predict wear-out time from thermo-mechanical induced stress.

Some of the most widely used models for lifetime assessment of power modules subjected to thermal or power cycling are the Coffin-Manson and Arrhenius expanded Coffin-

Manson models:[2, 8, 10]

$$N_f = A\Delta T_j{}^{\alpha}, \tag{2.1}$$

$$N_f = A\Delta T_j{}^{\alpha} \exp\left(\frac{E_A}{k_B T_{j,m}}\right), \tag{2.2}$$

where N_f is number of cycles to failure and α and A are constant factors describing the impact of ΔT_j. The Arrhenius term was added to incorporate effects induced from the mean temperature. As will be discussed in a following chapter, the theory behind the Coffin-Manson model structure is based on the assumption the damage goes within low-cycle fatigue approximations making it possible to separate the elastic and plastic deformation during thermal expansion . This leaves the ΔT as the sole stressor thereby motivating the model structure as in Eq. (2.1). The necessity for including the Arrhenius term in Eq. (2.2), however, indicates that the assumption is not completely correct. Several physical processes like diffusion, corrosion, etc. increases with the mean temperature. Accordingly, even though ΔT is within the low-cycle fatigue range it is not the only stressor.

Several expansions have been made of the Coffin-Manson model taking different contributions into account like frequency in the Norris-Landzberg model[56, 57], geometrical inputs like the Bayerer model[58], and models aimed more at specific designs, and interfaces.[2]. Especially, Uwe Scheuermann and Ralf Schmidt has done extensive work on constructing a detailed expansion providing a good estimation of expected lifetime under normal operation[11, 12, 59]. The latest is the SKiM63 lifetime model designed for that particular module design:

$$N_f = A\Delta T_j{}^{\alpha} \exp\left(\frac{E_A}{k_B T_{j,m}}\right) \cdot a_r{}^{\beta_1 \Delta T_j + \beta_0} \cdot \left(\frac{C + t_{on}{}^{\gamma}}{C+1}\right) \cdot f_{chip}, \tag{2.3}$$

where the first term is identical to the Coffin-Manson-Arrhenius model in Eq. (2.2), a_r in the second term is the wire bond aspect ratio with the exponent depending on temperature variation, the third term is a pulse duration modification with experimentally determined input parameters, and the fourth term (f_{chip}) is a modification term from chip thickness effects. Values for the different parameters are listed in [59]. The similarity between all models is its dependence on ΔT as main stressor and the need for end of life tests to determine the fitting parameters. While later models, like the SKiM63 in Eq. (2.3), has several component related inputs it requires a larger number of accelerated tests to provide reliable results. This is both expensive, time consuming, and in some cases still inaccurate with respect to life under normal conditions. This will be discussed in detail in Part III, but is related to the failure mechanism experienced under accelerated conditions not necessarily occurs or dominates under real life conditions. Furthermore, the obtained model is only valid for the particular component regarded. Meaning it has to be repeated for updated and new designs as well as similar devices.

An alternative to the pure empirical/statistical models more physics-of-failure based approaches have also been suggested. A balance between detail and computational effort is

essential to maintain usability in real life application. This has yielded suggestions like changing the Coffin-Manson model input to simple analytical derived plastic strain[43]. As well as more detailed plastic flow based analysis[15]. A concept being used more and more is to implement finite element method (FEM) based simulations of temperature distributions and mechanical stress into the stressor analysis[60–63]. While this significantly increase the understanding of critical areas in a power module, it is still often limited to only include a single wire bond or solder layer and is not necessarily directly implemented into the lifetime model.

Part II

Accelerated Testing and Characterization Techniques

CHAPTER 3

Accelerated Testing and Online Monitoring

The majority of samples regarded are tested using the wind power converter simulator presented in the following section. However, additional samples are regarded, see Sec. 1.2, these are stressed under normal accelerated conditions, like standard current loading, or comes from field use, see paper C.

3.1 Three-Phase Wind Power Converter Simulation

The setup presented in the following section is the accelerated test applied for stressing modules discussed in several papers, see e.g. E or G. The method is regarded as an advanced A-TC as the loading is not only a pulsed DC or current ramp, but an actively switched device. Apart from stressing power modules the setup is also designed to be able to test online monitoring solutions for assessing chip temperature and interconnection degradation. Setup maintenance, usage, and design is beyond the scope of this work; only relevance is to understand loading, monitoring methodology, and other parameters affecting component performance. Accordingly, only a limited description of the setup is presented here, for further information see papers D and E or [64, 65].

3.1.1 Test Setup

The setup is designed to simulate one leg in a three-phase wind power converter based on pulse width modulation (PWM). Accordingly, one device under test (DUT) is in operation at a time, see Fig. 3.1. For simplicity only the components circulating power is presented in Fig. 3.1 and all control/sensor components are left out.

The presented setup consists of a DUT, control side (CTRL) power modules, load inductors, and an external power supply delivering the fluctuating power and DC link voltage (V_{DC}). CTRL modules are used to control the direction of the load current (i_L) and thereby which elements of the DUT are active. A clear benefit of this setup is that the external power supply only needs to deliver the actual power loss of the setup components as the power is circulated.

Control of the load current decides which DUT parts are active, with $i_L > 0$ the high side (HS) IGBT (I_{HS}) and low side (LS) diode (D_{LS}) conducts, and similar with the control side. When $i_L < 0$ HS diode (D_{HS}) and LS IGBT (I_{LS}) conducts. This also illustrates the need of at-least two CTRL modules, given that they are identical to the DUT, as the CTRL

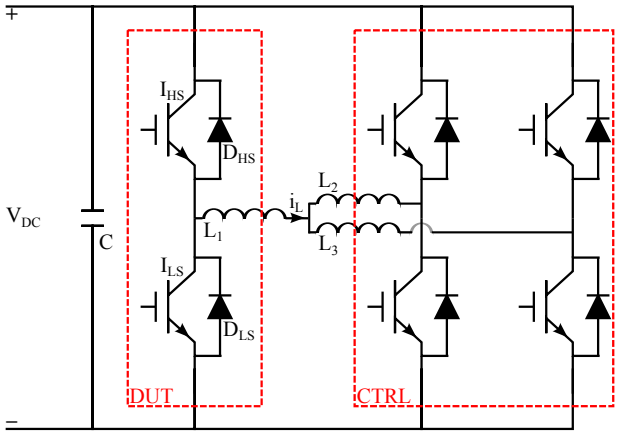


Figure 3.1: Schematic of the accelerated test setup applied in [7] and papers D,E.

part would fail together with the DUT. Inductors are included in this particular manner to ensure even load distribution between CTRL modules.

The DUT is cooled using direct baseplate backside cooling through Danfoss ShowerPower with a mixture of water and glycol, see [66]. Flow rate of the mixture is maintained as high as necessary to ensure constant cooling liquid temperature. The primary controlled stressors are the current amplitude (I_{tot}), the fundamental frequency (f_{out}), and the cooling temperature (T_{SP}). All relevant parameters are presented in Table 3.1:

Table 3.1: A-TC accelerated wear-out parameters.

Parameter	Symbol	A-TC
DC link voltage	V_{DC}	$1000V$
Phase displacement	ϕ	$2.7rad$
Peak load current	I_{tot}	$922A$
Fundamental frequency	f_{out}	$6Hz$
Switching frequency	f_s	$2.5kHz$
DC link capacitance	C	$4mF$
ShowerPower temperature	T_{SP}	$80°C$

3.1.2 Online Monitoring

Online monitoring of temperature sensitive electrical parameters is a used approach for avoiding catastrophic failures and to some degree a temperature sensor[64, 67, 68]. Efficient health monitoring is essential to avoid critical situations an predict failures. The chip

temperature measurement helps keep active devices within safe operation ranges[69], forward voltage can be used to detect overload or short circuits, as well as packaging degradation [22]. With regards to material degradation the parameters used in online monitoring are: v_{ce} (wire bonds), R_{th} (chip thermal path), and gate threshold voltage (gate oxide)[22].

Monitoring the on-state voltage of switching devices is problematic due to the signal scale compared to applied currents and switching voltages of power devices. Furthermore, when used as a degradation indicator variations in on-state voltage is on the scale of mV compared to V in absolute value[7]. So measurement precision, data management, and proper analysis is essential[19].

Monitoring Methodology

With the online measuring of forward voltage the possibility of monitoring changes and thereby component wear is possible. However, as illustrated in Fig. 1.2(a) the power module geometry is a complicated structure consisting of numerous layers/components. The obtained voltage is, if regarded as a series of linear resistors, a sum of the voltage drop across each individual layer/component. Thereby, effects from variation in production can have huge impact on data off-set as well as contribution weight. Furthermore, which individual part is displaying wear is difficult to obtain directly from the total potential difference. To overcome this, two different measure schemes are proposed ΔV_1 and ΔV_2:

$$\Delta V_1(n) = V_{P_1}(n) - V_{P_{ref}}, \tag{3.1}$$

$$\Delta V_2(n) = V_{P_2}(n) - V_{P_1}(n), \tag{3.2}$$

$$V_{P_{ref}} = \frac{1}{N}\sum_{n=1}^{N} V_{P_1}(n),$$

where n is the power cycle number, and N is chosen high enough to ensure a stable reference voltage ($N > 100$). P_1 and P_2 are the points specified in Fig. 3.2, where the $+$ and $-$ refer to the component side it is obtained on.

ΔV_1 specified in Eq. (3.1) clearly describes the change in forward voltage compared to the reference voltage. If N is chosen correctly this zeroes the signal in the beginning of the accelerated test and afterwards display the relative change. As will be displayed later on in Cha. 4, and is discussed in papers C and G, the primary contributor to changes in forward voltage is the bond wires and chip metallization[*1]. Accordingly, ΔV_1 primarily monitors changes in topside interconnects and increase in chip mean temperature.

ΔV_2 on the other hand is different. The measurements of V_{P_1} and V_{P_2} are carried out at the same load current $i_c = 900A$, but at the rise and fall of the half-cycle, respectively. Therefore, if conducted on an ideal system in complete steady state the result would be identical. However, in the time in between P_1 and P_2 work is performed on the sample by the applied load resulting in local heating. The resistivity of the metals and forward voltage of

[*1] Naturally, variation in the chip voltage drop is most significant, however, in the presently regarded load regime chip degradation is not expected.

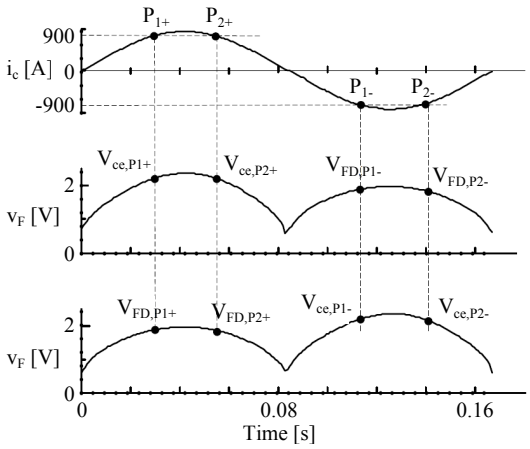


Figure 3.2: Online forward voltage for one power cycle, the chosen points are obtained at 900*A*. The figure is from paper E.

the semiconductor chips are temperature dependent meaning that $V_{P_2} > V_{P_1}$ [*2]. So in principle ΔV_2 gives a measure of degree of heating or resulting cooling between P_1 and P_2. The main heat path between chip and baseplate is through the solder which thereby is the primary contributor to changes in thermal impedance.

To summarize, ΔV_1 and ΔV_2 provide an online monitoring methodology able to separate chip topside (wire bonds and metallization) from bottom side (solder) degradation, from each other. Furthermore, as will be discussed in the following this enables removal of samples from operation prior to complete failure preventing catastrophic events and making pre-failure investigations possible.

3.1.3 Power Cycle Results

A number of samples were tested in the setup with the primary listed in Table 3.2. With a stable test system the initial sample (PM1) was power cycled until complete failure requiring 5.1MC. This was done to have a relative sample lifetime under the specifications listed in Table 3.1. Naturally, this is not an acceptable way to carry out lifetime estimation tests, but for now it is used to have a relative description of each sample.

Four other samples were tested to different stages in the relative lifetime - 4.5MC, 3.5MC, 2.5MC, and 1.3MC[*3]. All samples were monitored online while power cycling and measurements across the IGBT at P_{1+} and P_{2+} for PM1-PM4 samples are presented in Fig.

[*2]The main power-loss occurs in the chips, see Sec. 7.1, so the heating effects are most significant on the chip voltage.

[*3]As discussed in paper G this sample displayed very early changes in the forward voltage, and should as such not be compared directly to the remaining.

Table 3.2: Power module samples subjected to A-TC. The notation in column one and four refers to the notation applied in papers E and G, respectively.

Power Module	Number of A-TC	Condition	Abbreviation
PM0	0	Fabrication	A_{New}
PM1	$5103000 - 5.1MC$	Catastrophic failure	$F_{100\%}$
PM2	$4500000 - 4.5MC$	Operational	$E_{90\%}$
PM3	$3526200 - 3.5MC$	Operational	$D_{70\%}$
PM4	$2512800 - 2.5MC$	Operational	$C_{50\%}$
PM5	$1315800 - 1.3MC^{*3}$	Operational	$B_{25\%}$

3.3.

The earlier discussed difference in sample offset is clearly observed as well as the large

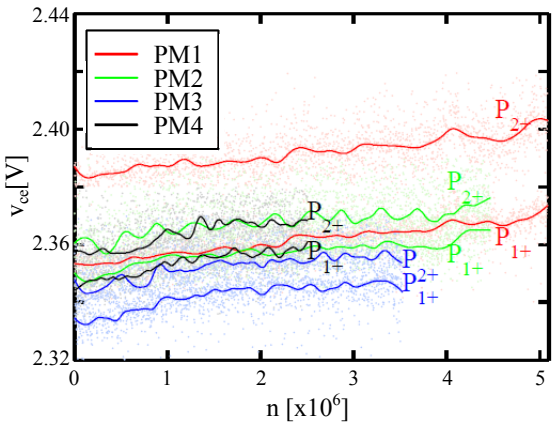


Figure 3.3: Online voltage difference at P_{1+} and P_{2+} across IGBT for samples PM1-PM4. Images is from paper E.

scale difference between absolute values and voltage increase. Additionally, the increase from P_1 to P_2 is seen to also display a small offset which is expected to be linked with the cooling liquid temperature, see paper E.

In Figs. 3.4 ΔV_1 are presented for the sample diodes. A clear tendency of the diode LS failing first is observed for the PM1 and PM2 sample. In the final part of the PM1 lifetime very large changes, resembling avalanche effects, are observed in ΔV_1. This is consistent with earlier reported results on forward monitoring, see [27, 53, 70, 71]. On the diode HS an increase is still observed but not on the same scale as the *LS*.

As illustrated in Fig. 3.4(a) the curves are separated into three categories - normal/fundamental wear, accelerated wear, and catastrophic failure. The first step is observed

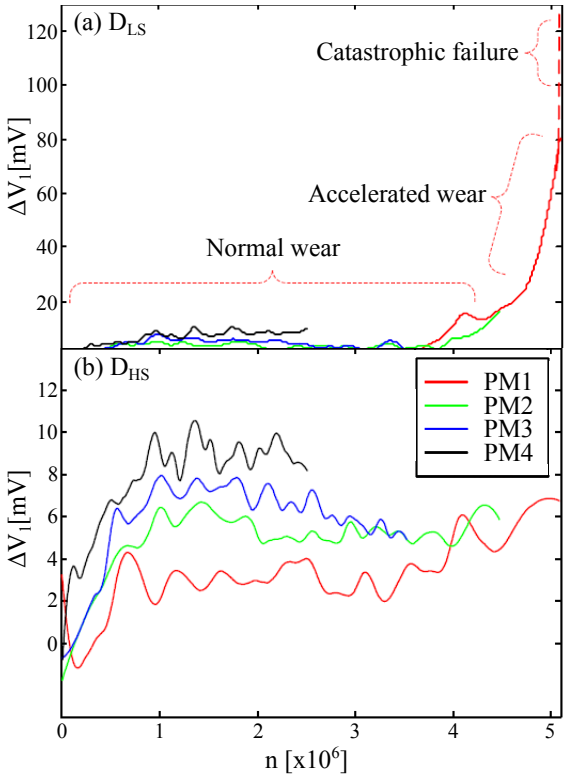


Figure 3.4: ΔV_1 for diode LS (a) and diode HS (b) as a function of number of cycles n. Image is from paper E.

on both LS and HS diodes with an early increase in ΔV_1 in the first *MC* for nearly all samples. This is attributed to the modules reaching a new quasi-static state after being placed into operation. Accelerated wear is only observed in the LS diode, which is due to geometrical effects. This is discussed in detail in Part III. Similar results, to the ones observed in Fig. 3.4(b), are available for the IGBT chips in paper E.

In Fig. 3.5 ΔV_2 is presented for the samples' LS diode. Apart from the offset of PM1 no notable increase is observed indicating limited solder degradation during the A-TC. The large variation in signal observed is mainly regarded as noise. One way to limit the noise effects is to increase the time between P_1 and P_2. When obtained at $i_c = 900A$ only a limited amount of relative heat-up is possible. By regarding the online voltage at $i_c = 700 - 800A$, where the chip temperature is still shown theoretically to increase in Sec. 8.1 the signal to noise ratio would be improved.

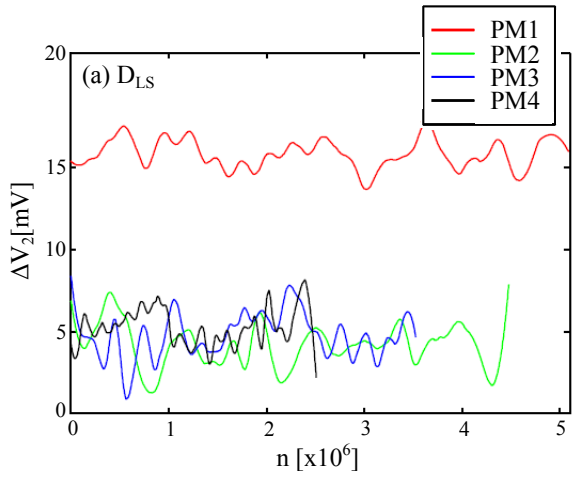


Figure 3.5: ΔV_2 for LS diode as a function of number of cycles n. Image is from paper E.

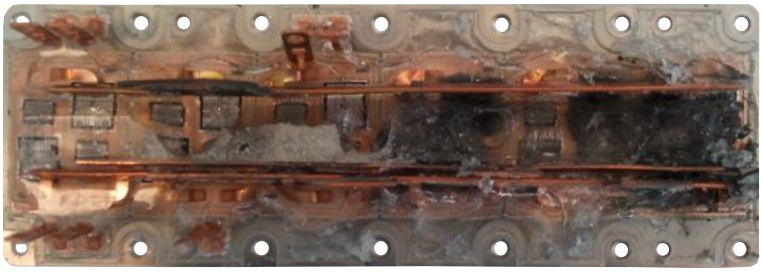
Preliminary Post-test Investigation

Preliminary post-test investigations are carried out prior to the detailed techniques presented in the following chapters. This is carried out during the initial steps of the micro-sectioning process described in Table 5.1. It is primarily a visual inspection recording macroscopic changes as illustrated for PM1 in Figs. 3.6.

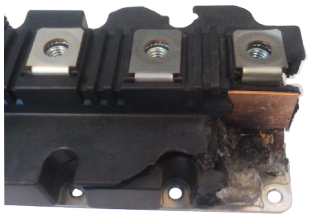
PM1 was stressed until complete failure which resulted in power module explosion, as seen in Fig. 3.6(b). While the explosion is observed as most severe around section 4-6 in Fig. 3.6(a) the majority of module chips (LS and HS) are no longer functioning. Section 3 is displayed without silicone gel in Fig. 3.6(c) where the majority of bond wires are seen to

have lifted. However, whether this is from fatigue or module explosion is unresolved. This underlines the necessity of online monitoring for failure investigation as well as avoiding catastrophic events.

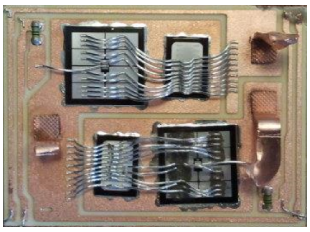
In Table 3.3 visual inspection results on the remaining samples are presented. Surprisingly, the sample displaying most drastic visual change is PM2. However, as indicated in PM4, production variation is also observed which could be a reason for the effects in PM2.



(a) Image of PM1 module without plastic housing.



(b) Exploded part of power module housing.



(c) Topographic image of section 3.

Figure 3.6: Preliminary post-test investigations of PM1 module, (a) before removal of silicone gel, (b) before removing plastic housing, and (c) section 3 after removal of gel.

Table 3.3: Preliminary post-test visual investigation of PM1-5.

Power Module	Section	Sub-component	Observation
PM1	All	-	Catastrophic failure
PM2	-	-	-
PM3	S1	D_{HS} wires 1 and 8	One bond lifted.
		D_{HS} wires 2-7	Wires lifted-off.
	S3	D_{LS} wires 1,6,7	One bond lifted.
		D_{LS} wires 8-10	Wires lifted-off.
	S4	D_{LS} wires 8-10	One bond lifted.
PM4	S6	D_{HS} wire 1	Bonding production error.
PM5	S6	D_{LS} wire 5	One bond lifted.

CHAPTER 4

Four-Point Probing

In this chapter the four-point probing approach for degradation assessment of power module interconnects is presented. By four-point probing an actual estimate of the present state of the individual elements of the power module can be obtained in a non-destructive manner. Results obtained through the method are presented in papers C and G.

4.1 Forward Voltage and Material Degradation

In Sec. 3.1.2 the concept of monitoring changes in the forward voltage for degradation estimation is presented. As illustrated in Fig. 1.2(a) the current path through a typical power module is across numerous layers, including the *Cu* pad, chip solder, semiconductor chips, chip metallization, bond wires, etc. Accordingly, which single or multiple elements are degrading is not distinguishable by the full voltage drop. On top of this the full power module normally consist of several sections acting in parallel to obtain high current capabilities.

Introducing a fracture, void, or foreign object into an interface is well-known to affect the voltage across the given interface[8, 22, 49, 51]. The concept of using the voltage drop as a degradation indicator is therefore applicable, one only needs to separate the individual components. By applying four probes, two current carrying and two voltage sensors, the potential difference across the probes are left out and only the voltage drop between the sensors are included. This is a common technique for high resolution measuring of local electrical properties[72, 73]. The necessity for this technique is twofold:

1. Sensors should not contribute to the final result.
2. Voltage drop across a full power module section is on the V scale where fracturing effects are on the mV scale.

In Fig. 4.1 a cross-sectional view of a bond wire/IGBT interface is presented. This illustrates the concept of using forward voltage as degradation parameter - the fracture decreases the effective bond area thereby increasing the effective resistance. The created difference is not only due to the reduced wire area but also the additional distance the current needs to travel inside the metallization.

The different measuring schemes applied in the present work are outlined in the following section.

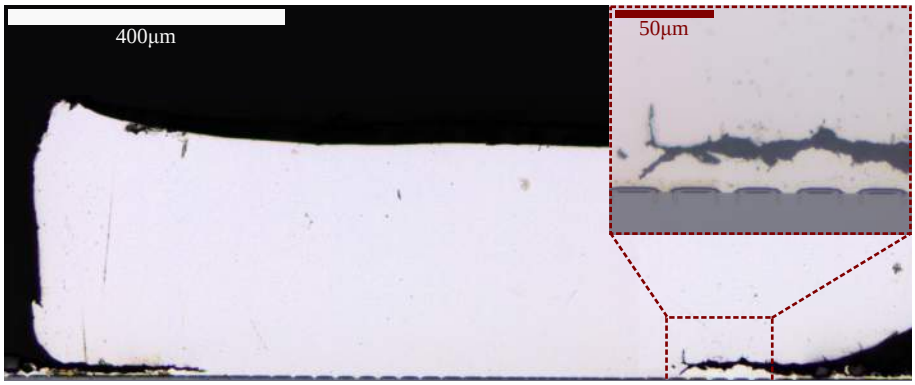


Figure 4.1: Cross-sectional view of wire bond on top of IGBT chip. The presented image is from paper C.

4.2 Four-Point Probing Setup

In order to measure the voltage drop across a given interface a sensor current (I_{tot}) has to be applied to the sample. This is applied through the section terminals as illustrated in Fig. 4.4(a)[*1]. The applied current is in principle only limited by the sample chip specifications, however, presently the sensor current is limited to $5A$ maximum. The motivation for this rather low current, compared to the regarded sample, is the purpose of investigating sample material degradation. No additional damage should be created and resistive heating in the sample only distorts the results. Furthermore, results are to be compared between different samples, therefore the substrate temperature needs to be maintained as stable as possible at a specified value. This is ensured in two steps:

1. Substrate temperature is controlled using proportional-integral-derivative (PID) control. The current applied to a series of Peltier elements are modulated using the relative difference between the ceramic surface temperature and the desired temperature. A thermocouple on top of the sample ceramic is used to measure the ceramic surface temperature, see Fig. 4.2.

2. The sensor current is applied in short pulses (t_{on}) with a pause in between (t_{off}) for sample cooldown. Forward voltage is measured after reaching steady state conditions ensuring a minimum of transient effects, see Fig. 4.3. The current is increased in steps of $0.2A$ from 0 to $5A$.

Ensuring everything is running in steady state is essential in order to rule out all capacitive and inductive effects of the regarded geometry.

In principle the gate voltage of the IGBTs as well as the substrate temperature could be

[*1] The placement of the voltage sensors is discussed in a following section.

varied similar to the sensor current to obtain additional data. In the presented data, however, only substrate temperatures of 40 and 50°C and a 15V gate voltage is used.

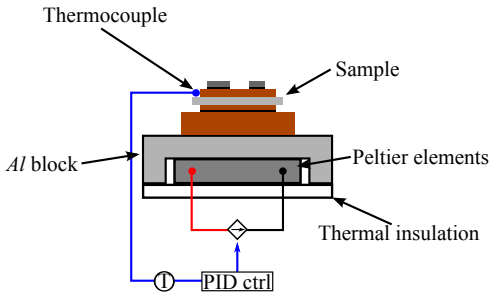


Figure 4.2: Schematic of the temperature control system in the four-point probing setup.

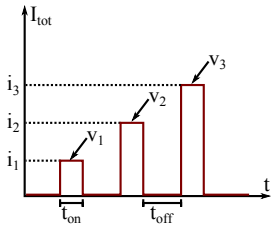


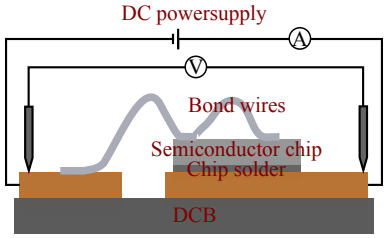
Figure 4.3: Pulse structure of applied sensor current.

4.2.1 Power Module Measuring Scheme

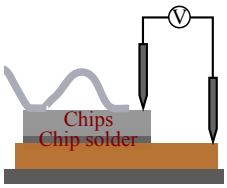
The power modules regarded are similar with regard to design and type of active components, see Sec. 1.2. Therefore a common measurement scheme is designed for all samples, with the primary ones outlined in Figs. 4.4. The three presented are referred to as terminal measurement (4.4(a)), chip measurement (4.4(b)), and bond wire investigation (4.4(c)). In all cases the current sensors are attached to the relevant section terminals as illustrated in Figs. 1.5. The presented examples are for the IGBT chips, but the approach is similar for the diodes.

Terminal measurements are simple in the sense that only one measurement is necessary as the importance of position of the two sensor probes on the terminal pads is limited. All subcomponents and layers are contributing to the signal, meaning that results are only viable for a quick view of section state.

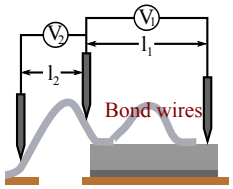
In chip measurements the sensor probes are placed as illustrated in Fig. 4.4(b) - one on the *Cu* pad and on the chip surface, respectively. Position of both probes are important with respect to comparing results between different samples and especially the chip surface probe is sensitive. The reason for this is the geometry and local state of the chip metal-



(a) Measurement between section terminals.



(b) Solder, chip, metallization voltage drop.



(c) Bond wire measurements.

Figure 4.4: Four-point probing measurement schemes on individual sections of regarded IGBT modules. The illustrated example is through the section IGBT chips.

lization. While the *Cu* pads and *Al* wires thickness is $300-500\mu m$ the *Al* metallization is only $4-6\mu m$. Meaning that small voids, flaws, cracks, etc. has a much larger impact on the measured signal. This is an advantage when investigating degree of degradation it also leaves the possibility to probe regions with singularities not necessarily representative for the entire chip. Therefore, several chip measurements are performed on each chip with the probe placed on several locations - four corners, side centres, and chip centre.

Wire measurements are the most complicated with respect to procedure. All regarded samples have more than ten wires in each power module section, leaving two options: measuring all wires together or on each individual wire. Both approaches are used, the initial one to asses if further measurements are relevant and the latter to single out degradation of individual wires. Measuring across all wires without chip included removes the IGBT v_{ce} out of the signal thereby increasing the resolution significantly. Measuring on each individual wire is separated into two steps: *(1) wire current distribution* and *(2) wire bond voltage*. These two are illustrated in Fig. 4.4(c). Obtaining the wire current is carried out by placing the probes with a known distance (l_2) in between on the wire curve and measuring the voltage difference (V_2). As the geometry in between the probes are well-known the current passing through wire i_w is derived from V_2. i_w can then be used to assess the current status of the wire bonds or the quality of the design. If combined with the voltage difference (V_1) from the wire heel to the wire curvature the effective resistance (R_w) of each wire may be derived.

4.3 Results

The presented four-point probing results are limited to the samples regarded in paper G. Additional results are seen in paper C. Only measurements on the bond wires are discussed in the thesis, additional results are available in the papers.

4.3.1 Wire Current Distribution

In Figs. 4.5 and 4.6 the relative wire current (i_w/I_{tot}) in the ten wires bonded to the LS and HS components of Fig. 1.5(b) are presented. I_{tot} is the current applied to the total section meaning i_w/I_{tot} is the fractional current in the given wire. The samples are, as discussed in Sec. 3.1, stressed additionally on the diodes meaning additional degradation are to be expected on these.

If one regards the distribution on the new samples in Fig. 4.5 the current is seen to

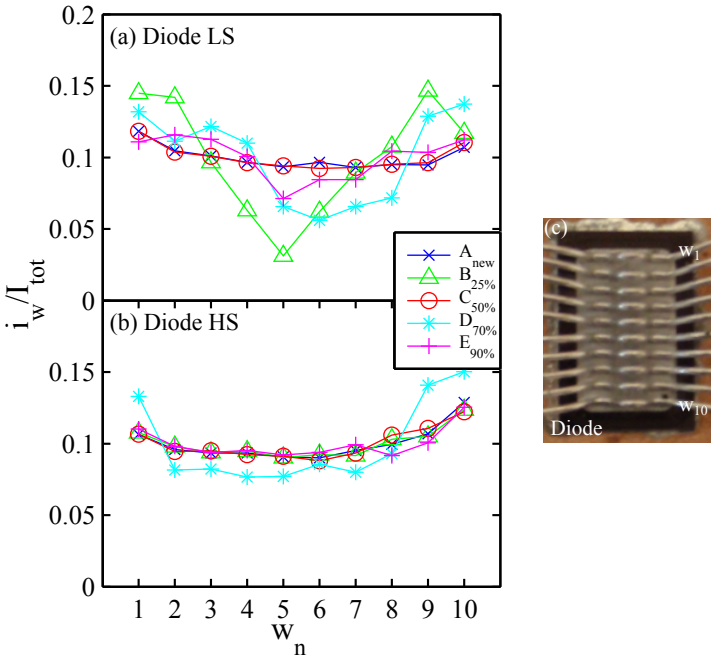


Figure 4.5: Diode wire current distribution of LS (a) and HS (b) together with topographic image (c).

behave according to geometry. An almost even distribution, except outer wires (w_1 and w_{10}), between wires is observed consistent with the even placement on the chip, see Fig. 4.5(c). The increased current in w_1 and w_{10} is attributed to the additional metallization area

available near the edge as well as lower temperature.

As expected selected samples, especially LS, are displaying wire bond wear. Centre wires are seen to carry a lower current after being subjected to A-TC which is consistent with thermo-mechanical simulations presented in a following chapter. Further discussion regarding actual degradation is carried out in the following section.

In contrast to the diode current distribution the IGBT clearly displays geometrical effects. Center wires ($w_4 - w_7$) are carrying additional current due to the increased metallization surface around the gate wire pad, see Fig. 4.6(c). Furthermore, the variation between the stressed samples and the new one is limited indicating either reduced or homogeneous wear.

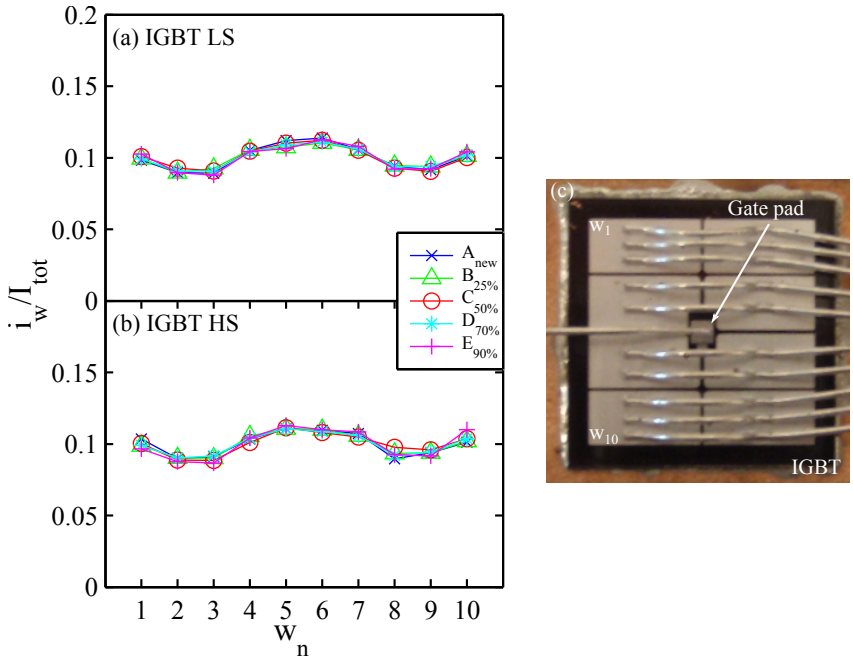


Figure 4.6: IGBT wire current distribution of LS (a) and HS (b) together with topographic image (c).

4.3.2 Change in Effective Resistance

By combining wire current with the voltage difference across the wire bonds an effective resistance is obtained, see Figs. 4.7 and 4.8.

Figs. 4.7 shows the change in effective resistance of the LS and HS side, respectively. A clear tendency of increased wear in the LS diodes are observed - resistance changes are in Ω compared to $m\Omega$ on the HS. It is presented in a following chapter that even though the test

setup is designed to place even loading between LS and HS, the LS diode is experiencing increased stress due to geometry. However, even when taking this into consideration the degradation pattern in Fig. 4.7(a) should still be proportional to the number of A-TC. The reason for the vast differences between wear and number of cycles is due to, as illustrated by singling out sample $D_{70\%}$-S_3, very severe damage on specific sections. These drastic differences observed are suspected to be related to fabrication variation, which with respect to thermo-mechanical degradation is known to have significant impact[8, 22, 59]. The severe impact is created by avalanche effects - if one wire is poorly bonded and lifts-off early all surrounding wires are stressed additionally. This is observed from wire to wire, chip to chip, and section to section. If one removes all sections (S_2-S_4) of $D_{70\%}$ displaying highly increased wear from the analysis, the change in effective resistance is below $E_{90\%}$[*2]. A similar situation is observed in the diode HS for the $C_{50\%}$ but at a much lower scale.

Change in resistance or degree of degradation of the IGBT chips' wire bonds are much

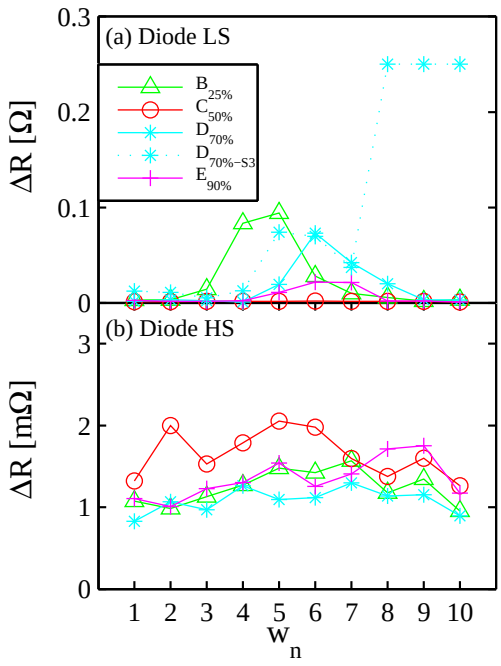


Figure 4.7: Change in effective diode wire resistance of LS wires (a) and HS wires (b).

more consistent with number of cycles. At the same time the degree of degradation between IGBT LS 4.8(a) and HS 4.8(b) are on the same level. The even degradation is consistent

[*2]The high impact from product variation clearly illustrate the necessity for a large number of samples, even when conducting micro-analysis.

with thermal simulations presented in Sec. 8.1.

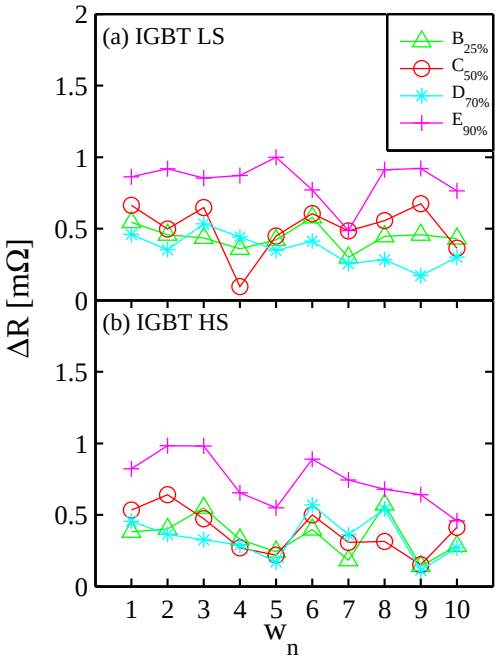


Figure 4.8: Change in effective IGBT wire resistance of LS wires (a) and HS wires (b).

4.4 Four-Point Probing Perspectives

The non-destructive nature of the characterization method opens up for possibilities regarding mapping of mechanical degradation patterns inside power modules. It is possible to conduct similar measurements as presented through the power module silicone gel and placing the component back into operation. This would enable a detailed mapping of the degradation field as a function of number of cycles/loading, thereby enabling the possibility to verify detailed degradation simulation. From the advanced modelling, geometry optimization would be possible as an alternative to accelerated testing in the early stages of the design phase. In the later stages testing are still essential in order to overcome the issue of fabrication variation.

CHAPTER 5

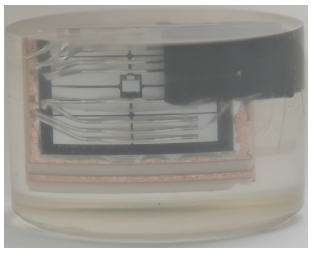
Micro-Sectioning

This chapter introduces the micro-sectioning approach developed for analysing present state of stressed power modules as well as quality and robustness of new devices. The method is primarily used for analysing wire/chip interfaces but could in principle be employed on any geometry. Results obtained through the method are presented in papers A, B, C, D, E, and G.

5.1 Cross-Sectional Analysis

In Sec. 1 basic layouts of IGBT modules are presented. These are complex structures consisting of numerous materials and sub-components. Accordingly, characterization of a given region/interface is complicated on many levels. A problematic often increased by the mechanical state of the regarded sample. With respect to investigation of failure mechanisms the samples of interest are in a damaged state prior to the characterization. This renders it necessary to place considerable effort in maintaining a steady state after beginning a given investigation.

Presently, the main interest is thermo-mechanical degradation of power module interconnects leaving the solder layers, metallization, and bond wires as the weakest elements. Based on this a method of obtaining cross-sectional views of the given interfaces are necessary to investigate the degradation process and the robustness of the components. This can be carried out using advanced equipment, like focused ion beam (FIB), but with limited investigation area and problems with layered structures like the transition from ceramic to *Cu*. Instead, large scale investigations are based on a simple micro-sectioning approach centred on: *(1) embedding the sample in epoxy for protection (see Figs. 5.1), (2) mechanical removal of unnecessary parts, (3) mechanical grinding until reaching desired interface, (4) fine grade polishing,* and *(5) optical microscopy*.



(a) Top view of IGBT chip embedded in epoxy.

(b) Side view of IGBT chip embedded in epoxy.

Figure 5.1: IGBT chip on top of DCB substrate cast in epoxy. Images are from paper A.

5.1.1 Bond Wire Grain Structure

In Secs. 1.1 and 2.2.1 bond wire interconnects as well as the concept of bond wire related failure mechanisms are introduced. Here it is discussed that the microscopical structure of the *Al*-wire/chip interface and its robustness is directly coupled. More precisely the granular structure of the metallic connection is an important factor in its strength. The reason for this is most easily described through fundamental fracture mechanics, see Sec. 7.4, for now, however, we merely accept that knowledge regarding the microscopical structure is needed.

Obtaining the grain structure of pure *Al* in a layered system is problematic, as the contrast in the *Al* is often caused by impurities. The missing contrast across the *Al* is further lowered by the surrounding layers in the geometry. Therefore, mechanical separation of the relevant components as well methods like electron backscattered diffraction (EBSD) and electrochemical etching may be employed to visualize the change in crystal structure.

Color Metallography

Natural occurring differences in color on smooth polished pure metal surfaces is not a commonly observed phenomena using standard optical techniques. Multiple techniques for promoting color contrast on the surface exist based on both microscopy techniques and additional surface treatment.[74, 75]

With respect to characterization technique the present introduction is centred around optical microscopy- and scanning electron microscopy (SEM) methods. The four main techniques applied in standard optical microscopes are based on: *(1) bright field, (2) dark field, (3) interference contrast,* and *(4) polarized light*. All mentioned techniques, except the one based on polarized light, can be carried out on standard purely polished surfaces. However, in these cases the color contrast between grains or across grain boundaries are created by strong non-isotropic changes. With the use of polarized light the metal surface needs to be subjected to an anodization prior to investigation. When regarding pure *Al* and many *Al*-alloys the latter approach is preferable[76–78]. With regard to SEM numerous approaches for examination of crystallographic structure and composition exists. In the present work

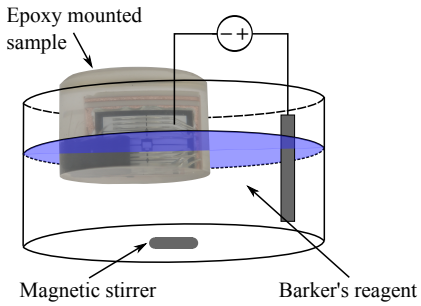


Figure 5.2: Illustration of the electro-etching setup.

only standard SEM techniques like secondary- and backscattered electron images combined with FIB and EBSD are considered. In all cases, however, the imaging are often limited by the scale of the equipment. FIB milling across a *mm* thick interface is not ideal, accordingly, a combination of mechanical treatment, optical analysis of full sample, and SEM investigation of specific regions is the ideal approach.[74, 75]

Anodization of *Al* Surface

Anodization of smooth pure *Al* is an electrolytic process increasing the thickness of the natural metal oxide. Normally, the oxide growth is epitaxial making the process ideal for investigation of grain structure under polarized light. The most commonly used solution for pure *Al* and *Al*-alloys is the so-called Barker's reagent combined with a potential difference. Barker's reagent is normally mixed with $10ml$ fluoroboric acid (HBF_4) (35%) in $200ml$ water. The etching time and voltage difference in the electro-etching depends on the situation, presently the samples are etched for $2-3$ minutes with $20-30V$ depending on sample, see Fig. 5.2.[75, 76]

5.2 Experimental Procedure

The procedure described in Table 5.1 depends highly on the regarded module and interface of interest. The presented approach is designed to reach the bond wire/chip interface of the module introduced in Fig. 1.2 and Table 1.1. In order to regard another interface or module type the procedure should be modified accordingly.

Table 5.1: Step-by-step description of the experimental procedure in the power module disassembly process. During step *a-1* preliminary post-test investigations are conducted and prior to step *a-4* any four-point probing measurements are carried out.

Step:	**Procedure:**
(a) Baseplate removal	**(1)** Remove plastic housing without pulling silicone gel away from surface elements. **(2)** Separation of parallel sections by cutting of baseplate in between. **(3)** Dissolve silicone gel. **(4)** Embed sections into epoxy for sample protection. **(5)** Removal of baseplate from section by horizontal cutting in parallel with DCB.
(b) Sub-element division	**(1)** Vertical cutting through DCB for separation of IGBTs, diodes, etc. **(2)** Re-embedding of sub-elements into epoxy.
(c) Chip/wire isolation	**(1)** Grinding from the backside of the DCB and upwards toward the chip interface. **(2)** Remaining *Cu* and baseplate solder is removed using rough grade *SiC* paper. **(3)** Ceramic is removed using a diamond based dish. **(4)** DCB upper *Cu* layer and chip solder is removed using fine grade *SiC* paper.
(d) Wire/chip interface	**(1)** Rough grade *SiC* paper grinding until reaching chip side. **(2)** *SiC* paper polishing until reaching wire/chip interface of interest. The paper roughness is decreased in steps until reaching the interface. **(3)** DiaDuo $3\mu m$ diamond suspension polishing for removal of *SiC* paper polishing lines. **(4)** OP-U - $40nm$ colloidal silica suspended particle polishing. **(5)** Electro-chemical etching of interface for grain structure visualization.

Throughout the entire process one should keep in mind the problems connected with handling layered structures. The *Al*-wire, for instance, has a much lower hardness than the *Si*-chip or cast epoxy. Accordingly, the risk of embedding either foreign elements or residue from the surrounding layers into the *Al* is significant. These elements should be removed prior to the final steps in the polishing process.

5.3 Results

Application of the micro-sectioning procedure listed in Table 5.1 was primarily used for two purposes: bonding optimization and bond wire degradation investigation. Additionally, reconstruction effects in the chip metallization were investigated prior to embedding in epoxy.

5.3.1 Wire Bonding Optimization

To investigate the possibility of optimizing the standard US bonding process only by microstructural investigation a series of test samples were fabricated. Two types of pure (99.99%) *Al* wire (A and B) were regarded each bonded to a standard IGBT module section layout, see Fig. 1.2(b), with three power settings. To summarize this means that six different fabricated sections were regarded ($A_1 - A_3$ and $B_1 - B_3$) were each section contained three types of bonded wire interfaces: *(1) on top of the Cu-pad, (2) diode,* and *(3) IGBT*. To validate the obtained results standard shear tests were performed on identical samples for comparison. Shear test results as well as a detailed fabrication description are presented in paper B.

A clear tendency of a relation between initial wire structure, bonding parameters, and bond quality was evident. This is as would be expected by considering the bonding process as described in Sec. 1 [28–32]. The fundamental difference between wires A and B was clear from grain structure analysis of the wire outside the bonding region. This is partly illustrated in 5.3(a) and 5.3(b) which display cross-sectional images of the wires near the initiation the wire/chip bond.

The structural difference observed between wire type A and B is related to the grain structure in both size and distribution. In wire type A large grains ranging from 10 to 70μm is observed with the size depending on position - grains near the wall are smaller than at the centre. In contrast the grains in wire type B are only 5 to 20μm in diameter and are homogeneously distributed with respect to size. This initial difference in wire structure changes the US bonding process as the wire hardness is governed by the grain size through the Hall-Petch relation[79], see Eq. (7.47). Recrystallization of the structure into smaller grains is also the main purpose, as discussed in Sec. 1.1.1, in order to create a refinement area on top of the chip with a high yield strength.

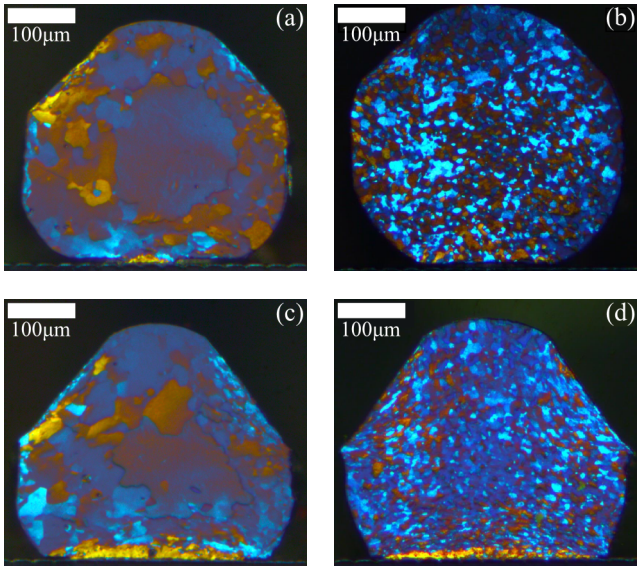


Figure 5.3: End-view images of samples A_3 and B_3 close to the initiation (5.3(a) and 5.3(b)) and around the middle (5.3(c) and 5.3(d)) of a wire/IGBT interface. Images are from paper B.

In Figs. 5.3(c) and 5.3(d) end-view cross-sectional images are presented of the same samples but closer to the bond centre. In contrast to the cross-sectional images near the bond initiation the bonding process has affected the wire structure significantly. Refined areas are observed near the wire/chip interface. An oval structure is observer, i.e. deeper refinement in the wire around the middle and more shallow at the edges. This is consistent with the bonding approach presented in paper B. The refined area of sample A_3 appears larger than in B_3 in the presented images, however, this effect is primarily created by the large difference between bulk grains and refined grains. In Fig. 5.3(d) the transition from a refined region to what could be referred to as a bulk region is gradual whereas in Fig. 5.3(c) it is more abrupt. Which situation is ideal depends highly on the component application, and thereby the experienced stress by the interface. While an abrupt transition from refined to bulk grains is an ideal region for crack propagation the load itself has to high enough to reach the region and travel. Similarly, the gradual transition provides many possible propagation regions without any of them being between critically large grains.

End-view cross-sectional images were obtained on all samples for many interfaces. A clear connection between applied power and refinement area height was obtained thereby explaining the difference observed in the shear test. Furthermore, by obtaining several cross-sectional images of the same wire/chip interface, with a given distance in between, a 3D reconstruction of the refinement region, as well as the wire deformation, was constructed.

This is discussed in detail in paper B.

Structure of the refinement region as well as the wire deformation is illustrated in Fig.

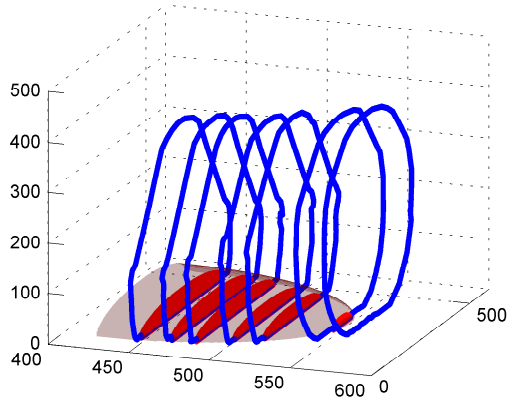
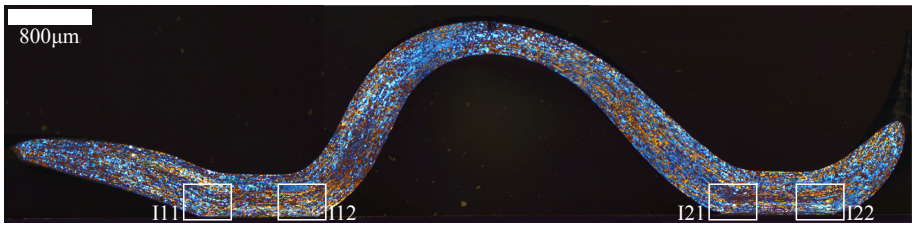


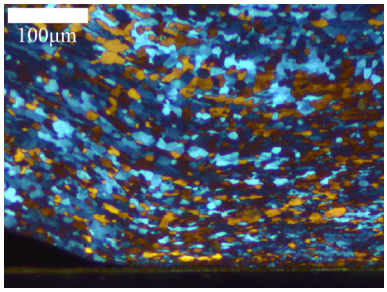
Figure 5.4: 3D reconstruction of a B_1 wire/IGBT interface, the grain refinement region approximately spans half an ellipsoid. Figure is from paper B.

5.4. The ellipsoidal shape of the refined area is in accordance with the observed residue left from the shear test and earlier studies in bond footprints [29]. Similarly, the outer wire shape is in accordance with the plastic flow occurring during bonding.

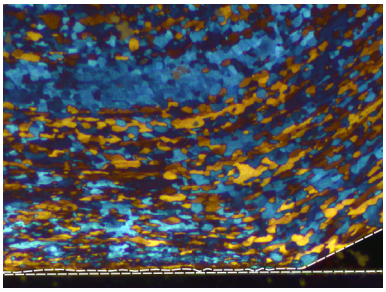
End-view cross-sectional images provide a strong investigation of the refinement region as well as the wire deformation. However, fractures are normally initiated near the bond heel or toe[25, 43, 80]. This is linked with the wire/chip interface termination being a natural crack initiation site. So a proper closure of the bonding process could be as significant as small grains in the refinement region. In Fig. 5.5(a) a side view cross-sectional image of an entire bond wire curve on top of a diode is presented. The grain structure is visible for the entire curvature giving a strong impression on the plastic deformation occurring during bonding. Together with the wire cross-section, enlarged images of the bond termination is provided for both interfaces, see Figs. 5.5(b)-5.5(e). Even though identical bond parameters are used for both interfaces in the fabrication a clear difference in bond termination is observed. This is believed to be created by the stepwise bonding process commonly used. In papers C and F it is shown experimentally and theoretically that the stress and therefore degradation level on the different power module wire bonds are not identical. A problematic which could be further complicated by imperfect bond termination.

To summarize, the bond optimization process through micro-sectioning analysis showed that a number of parameters affect the bond quality: material composition and structure of original wire, US bonding parameters, steps in the bonding procedure in between bonds.

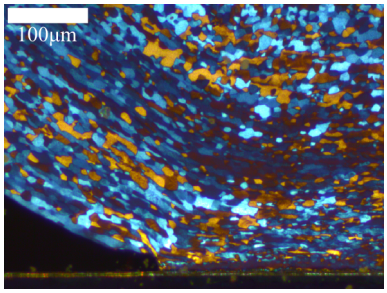




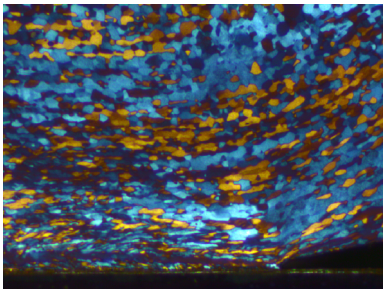
(b) I11



(c) I12



(d) I21



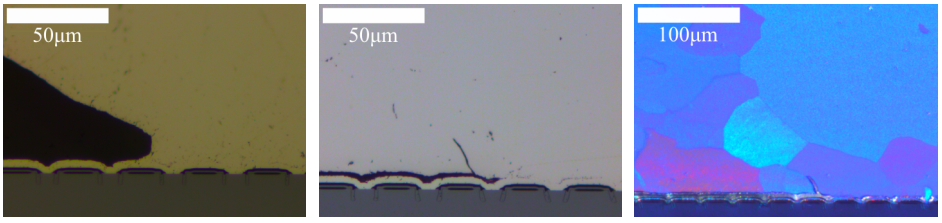
(e) I22

Figure 5.5: (a) Side view cross-sectional image of wire curve on top of a diode from B_3. (b-e) Magnified images of the interface corresponding to the inserts shown in 5.5(a). Dashed line in panel (c) is given for better visualization of the junction between the wire and metallization. See text for details. Images are from paper B.

5.3.2 Bond Wire Fatigue

Bond optimization based on interface characterization of new samples can only be used to increase the absolute bond strength and assess the probable fracture path. With regard to fatigue bond strength and the actual fracture path as a function of load one needs to characterize samples stressed under the given conditions.

In Figs. 5.6 three cross-sectional views of wire/IGBT interfaces are presented. Fig. 5.6(a) displays a new sample from B_1 with a terminated bond which should reduce the fracture speed. In contrast Figs. 5.6(b) and 5.6(c) show a wire/IGBT interface from $F_{100\%}$ which did not have the same bond termination and after being subjected to A-TC displays clear tendencies of delamination. The images are obtained at the same position, as indicated by the fracture, before and after the sample was electro-etched. Without electro-etching the delamination process is observable, but without actual knowledge of the fracture path. Applying electro-etching and polarized light in the characterization reveals much more detail regarding the wire lift-off. In this example the grains near the chip surface are not refined significantly indicating a poorly bonded wire, see Sec. 5.3.1. The fracturing is observed to occur between chip and grains, and not inside the wire itself. An example of the initiation of a vertical propagating fracture is illustrated but its direction and that the delamination has passed it indicates it is not likely to continue if the sample was placed back in operation. Furthermore, in Fig. 5.6(c) the actual length of the delamination process is more clear than in Fig. 5.6(b) due to the contrast provided under polarized light.



(a) Ideal IGBT *Al* wire bond. (b) IGBT bond wire from $F_{100\%}$. (c) Sample 5.6(b) etched.

Figure 5.6: Example of failure analysis using micro-sectioning approach with and without electro-etching. Images are from paper A.

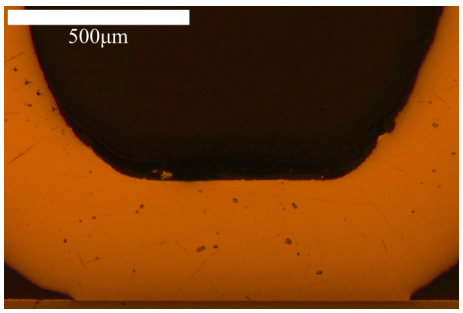
Bond Wire Lift-Off in A-TC Power Modules

As introduced in Sec. 3.1 an accelerated test setup simulating wind power converter conditions was build and used for stressing a number of power modules, see Table 3.2. In the given samples a clear tendency of wire lift-off related failure mechanisms was observed in nearly all samples, see Sec. 4.3 and paper G for additional details.

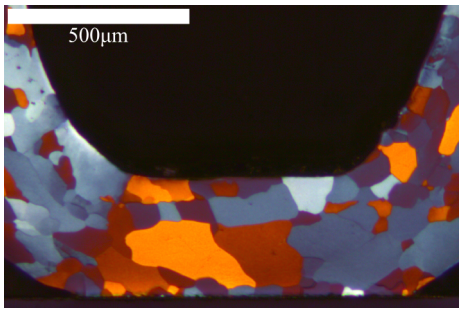
In Figs. 5.7 three cross-sectional images of wire/chip interfaces are presented. Fig.

5.7(a) shows a stitch bond on top of a diode from A_{New}. The bond termination is not as ideal as observed in Fig. 5.6(a) but more like in Fig. 5.5(c) which is an ideal source of fracture initiation. Similar images are presented for a stitched bond on top of a diode 5.7(b) and an IGBT 5.7(c) but after electro-etching. The difference in the wire curve after the stitch bonds displayed in the figures are another clear source of unnecessary stress. After diode bonds the wire is observed to rise significantly steeper than at IGBT bonds. This has been shown to directly affect the wire bond lifetime[45, 80].

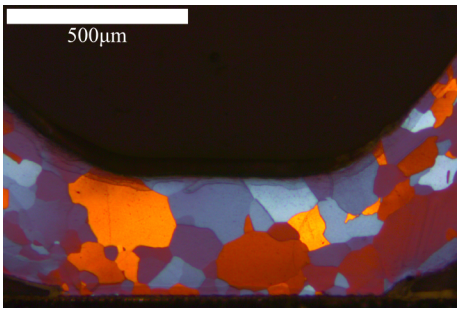
Compared to optimized samples as discussed in Sec. 5.3.1 the *Al* grains are extremely



(a) Wire/chip interface on the diode of A_{New}.



(b) Wire/chip interface on the diode of A_{New} electro-etched.



(c) Wire/chip interface on the IGBT of A_{New} electro-etched.

Figure 5.7: Wire/chip interfaces on top of diode (a)-(b) and IGBT (c) from a new power module (A_{New}).

large. This has a direct impact on the wire lift-off process as illustrated in the following figures. Figs. 5.8, 5.9, and 5.10 presents cross-sections of wire/chip interfaces of IGBT end bonds from samples $C_{50\%}$, $D_{70\%}$, and $E_{90\%}$, respectively. In all figures the wire lift-off process is observed as a hybrid of wire delamination and actual intergranular fracturing. In Fig. 5.8 a significant part of the wire bond is already fractured and the crack is seen to move close to the chip surface. But the fracture is primarily seen to move between grains or intergranular as would be expected. However, when regarding samples subjected to a higher

number of cycles, see Fig. 5.9 and 5.10, the fracture path is seen to move within grains, or transgranular, as well. In both interfaces the bond degradation process is close to wire lift-off and especially $E_{90\%}$ displays many transgranular fractures.

All-in-all the wire fatigue observed in the samples are consistent with the wire bond

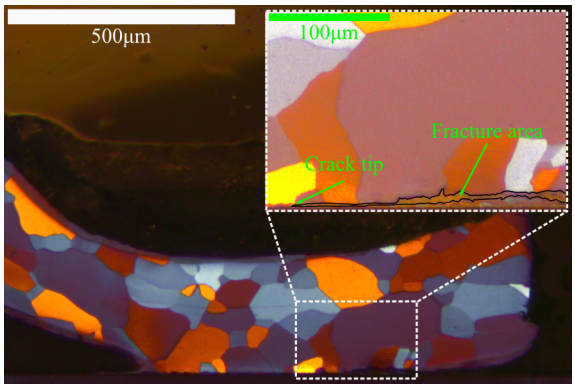


Figure 5.8: Wire/chip interface of end bond on IGBT from $C_{50\%}$. The insert illustrates the fractured area and the position of the crack tip.

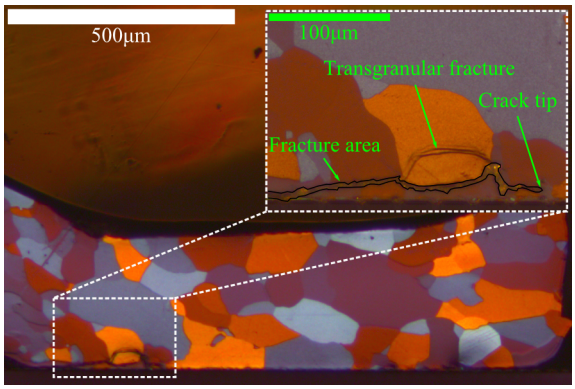


Figure 5.9: Wire/chip interface of end bond on IGBT from $D_{70\%}$. The insert illustrates the fractured area, position of the crack tip, and an transgranular fracture.

quality in the new samples. The large grains makes the fracture propagate close to the chip surface, and not inside the wire itself as would be preferred. Furthermore, the grains are of so large a diameter that the fracturing tends to occur transgranular at later stages in lifetime.

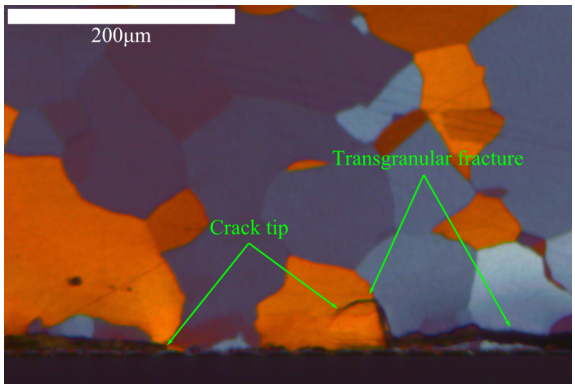
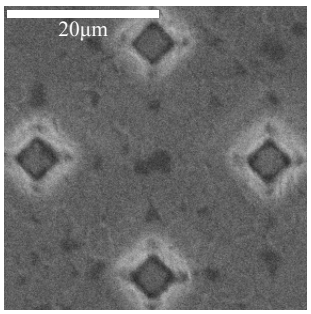


Figure 5.10: Wire/chip interface of end bond on IGBT from $E_{90\%}$. A large number of transgranular fractures are observed.

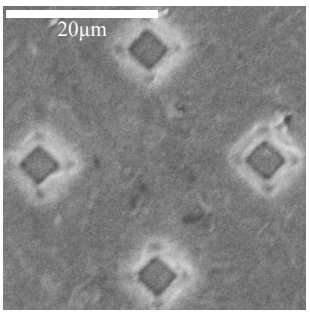
5.3.3 Metallization Reconstruction

Prior to embedding the samples regarded in Sec. 5.3.2 in epoxy the chip metallizations were investigated using SEM imaging and FIB milling. The power cycling load was designed to stress the diodes most severely which is also apparent in the state of the metallization. Under the conditions experienced by the IGBTs no metallization damage are observed, see Figs. 5.11(a) and 5.11(b):

On the diodes, however, severe reconstruction effects were observed on both LS and HS



(a) Topographic SEM image of IGBT from A_{New}.



(b) Topographic SEM image of IGBT from $E_{90\%}$.

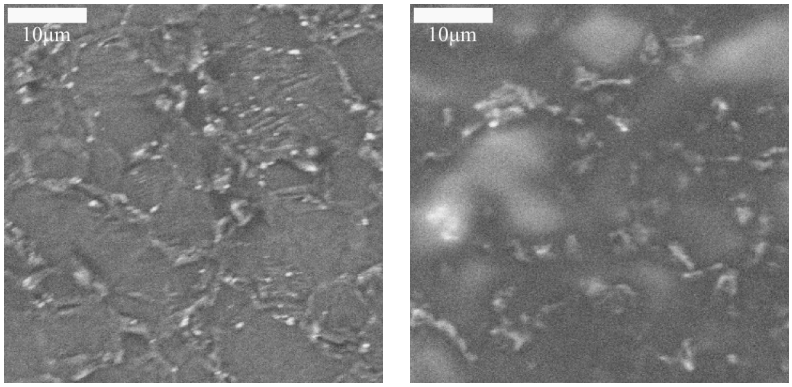
Figure 5.11: IGBT metallization images from (a) A_{New} and (b) $E_{90\%}$.

chips. Furthermore, there was a clear difference between degree of degradation near the chip centre and the edge. In Figs. 5.12 topographic images of the metallization obtained by SEM is presented near the edge *(a), (c), (e)* and near the centre *(b), (d), (f)* on LS diodes from

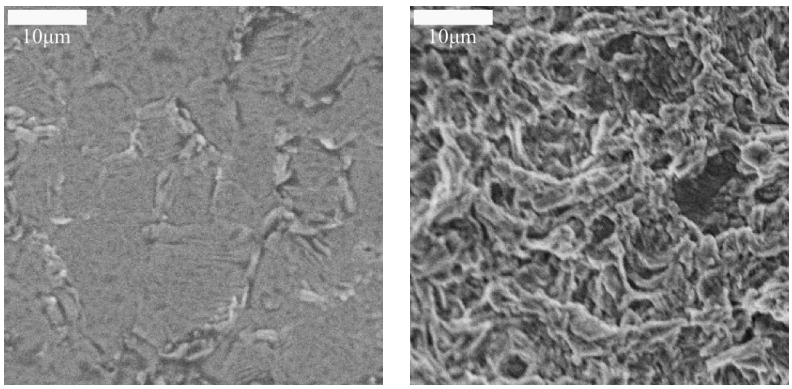
$C_{50\%}$, $D_{70\%}$, and $E_{90\%}$, respectively. Degree of reconstruction is not distinguishable between LS and HS components.

The difference between edge and centre images, as well as the degree of degradation being proportional to number of cycles, is consistent with metallization reconstruction being a thermally induced low-cycle fatigue process. This is discussed in detail in Cha. 7.1. Near the end of the module lifetime the metallization is observed to be in a sheet like structure instead of a solid film. This could be a critical situation with either highly reduced film thickness or loss of contact to parts of the semiconductor.

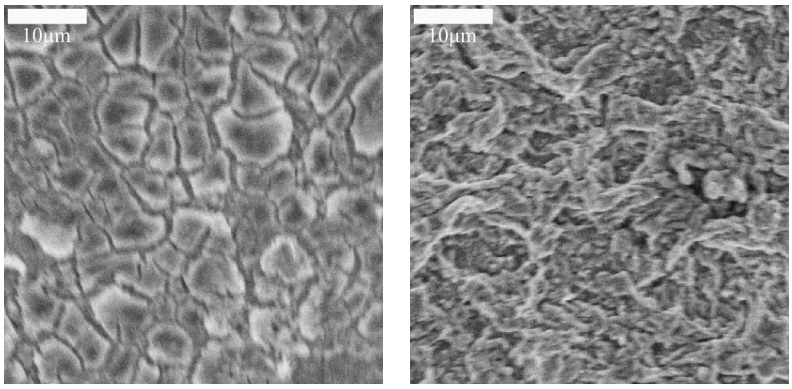
In Fig. 5.13 FIB milling has been employed to create cross-sectional images of the metallization to investigate the vertical reconstruction effects. A clear increase of cavity depths are observed when increasing number of cycles or when comparing chip edges to centre. The reconstruction process appears solely thermally induced. No sign of electro-migration or severe diffusion processes are observed. However, this is not conclusive, additional tests without current loading are needed.



(a) $C_{50\%}$ LS diode edge. (b) $C_{50\%}$ LS diode centre.

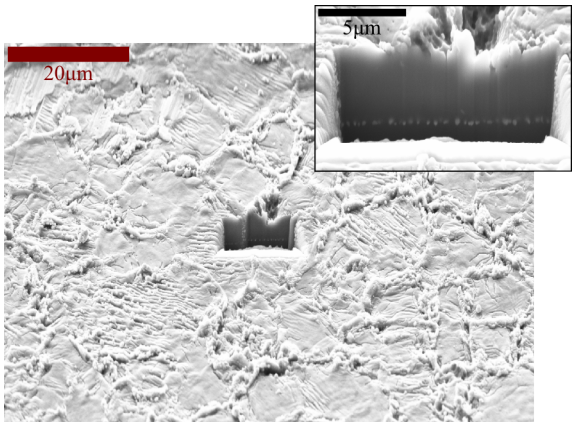


(c) $D_{70\%}$ LS diode edge. (d) $D_{70\%}$ LS diode centre.

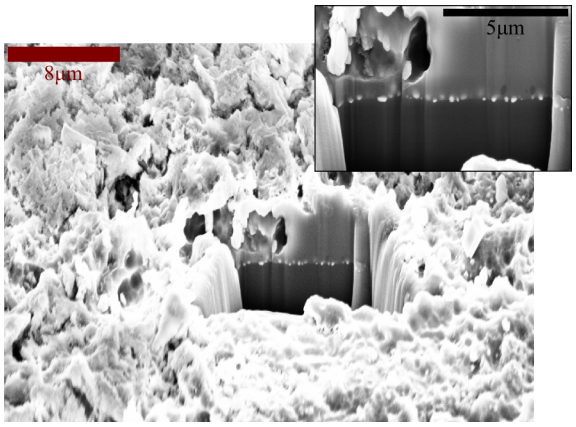


(e) $E_{90\%}$ LS diode edge. (f) $E_{90\%}$ LS diode centre.

Figure 5.12: Diode metallization surface SEM images of A-TC samples.



(a) $C_{50\%}$ LS diode centre.



(b) $E_{90\%}$ LS diode centre.

Figure 5.13: Diode metallization SEM/FIB cross-sectional images of A-TC samples.

Part III

Degradation Modelling

CHAPTER 6

Dynamic Modelling Approach

As presented in Sec. 2.4 the most commonly used model for lifetime estimation of package related failure mechanisms in power modules has been based in the Coffin-Manson model, see Eqs. (2.1)-(2.3).

The simplicity of the models are both an advantage and disadvantage. In principle they can be applied to any element failing from thermo-mechanical induced degradation, however, one needs to obtain component specific parameters from fitting to test data. In high power electronics the expected component lifetime often exceeds 10 years, accordingly, one needs accelerated conditions to obtain lifetime information within a reasonable time frame. This is also the commonly used approach, as presented in Sec. 2.4. Component performance at normal operation is then obtained by data extrapolation. While this approach has been useful for more than a decade, it has begun to be problematic in recent years. There are several reasons for this:

1. The simplicity of the model does not take into account the effect of the geometry and material composition. These effects have to be obtained through the fitting parameters. It has been reported that changes of e.g. wire curvature alone as well as bond footprint affect the lifetime directly.[80, 81]

2. With ΔT as only input parameter and only one set of fitting parameters attached to the stressor the model assumes the eventual failure is either a single mechanism or a series of mechanisms connected to ΔT with a constant grouping.

3. Failure mechanisms observed under accelerated conditions are not necessarily occurring at normal operation.

4. Variation in production quality requires a very large quantity of wear-out tests.[59]

The first problematic has in later years been sought solved by increasing the number of fitting and input parameters in the same way the Arrhenius factor was added in Eq. (2.2), see [12, 14, 59]. However, this still only delivers a functioning lifetime model at accelerated conditions as well as for the particular module tested. In the following section the overall idea and structure of the proposed degradation model is presented.

6.1 Model Structure

In principle all degradation models in cyclic systems are based on the same steps: *load, damage, recovery*. These process steps run simultaneously and continue to do so until reaching a given failure condition. In the present situation the regarded problem is electro-thermo-mechanical degradation of interconnects in high power IGBT modules. To construct a degradation model for this system one need to understand the load conditions, relevant sub-components, and degrading elements. The power modules of interest are primarily used for power conversion in high power application fields, e.g. wind mills or automotive. Based on this the model presented in Fig. 6.1 is proposed.

Due to the complexity of the regarded system, the model is as far as possible sought divided into steps. In Fig. 6.1 four primary sections constitute the model: *(1) power loss, (2) temperature field, (3) solid mechanics,* and *(4) material degradation*. These are all interconnected as partly illustrated by the lines in the flow chart. This may be explained by regarding an interface between to arbitrary conducting materials subjected to a pulsed DC current. With the current running both materials are heated up due to resistive losses and materials expand. With a CTE mismatch a stress is induced in the interface which over time may cause material damage due to stress relaxation. This affects the current distribution and thereby the power loss etc.

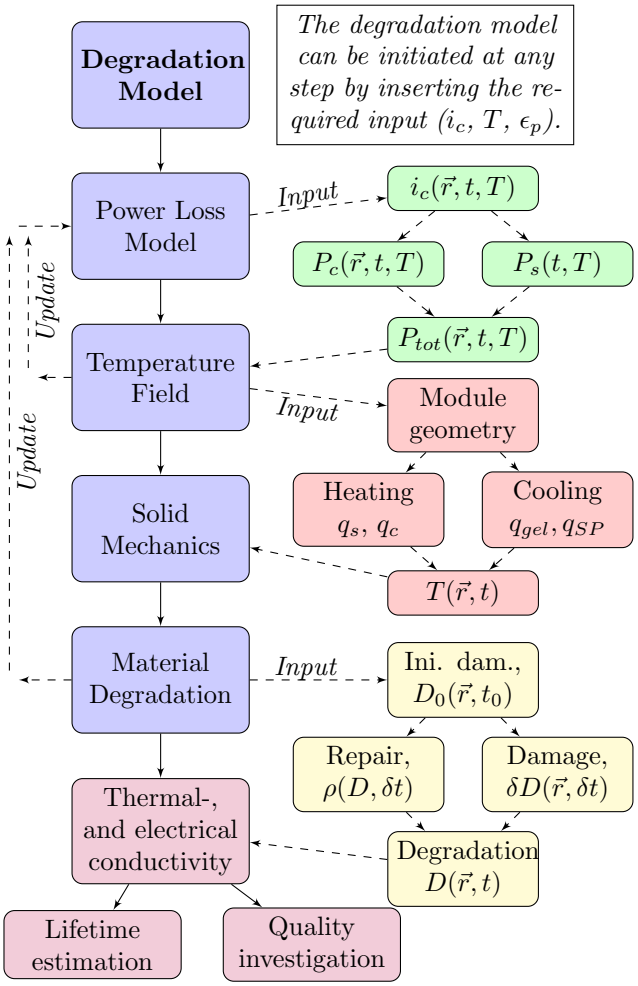


Figure 6.1: Flow chart of electro-thermo-mechanical degradation model of power module interconnects.

If one expands the two layer model to regard a full component in real life application the before mentioned example is too simple. This is sought illustrated in Fig. 6.1 with the secondary branches. Compared to the two part slab the geometry of interest is no longer only passive components. Instead several active elements affect the current distribution. Based on this the power loss is no longer only conduction losses but also semiconductor switching losses, blocking losses, etc. Furthermore, all power loss calculations are highly temperature dependent linking step *(1)* and *(2)* closely in the model. The thermal modelling is simi-

larly complicated. Under operation power modules are actively cooled down to limit power losses, in high power applications this is normally done through backside water cooling or by attaching a heatsink. Apart from the actively cooled parts the remaining geometry is passively cooled by the surroundings. All this affects the current distribution, the power loss, and resulting temperature field. Meaning all electro-thermal simulations are to be repeated until converging towards a steady cycle. From the temperature field the thermo-mechanical simulations can be carried out. These are based on a standard structural mechanics approach combined with a degradation model to account for microscopical fracturing processes. Once again this links to previous simulations: fractures affect the current distribution directly and thereby cause a new steady cycle level in the electro-thermal simulations. With these considerations in mind the model process and possibilities is explained in the following section.

6.2 Model Application

The model depicted in Fig. 6.1 should be applied depending on desired outcome. A full-scale analysis of the current distribution, power loss, temperature field, structural mechanics, and material degradation for end of life simulations is highly time consuming due to computational demand. If the goal is to optimize the geometry layout or identify possible critical areas only a limited time period should be simulated. However, if a lifetime estimation or large time period is to be considered, simplifications should be implemented. Suggestions to model applications are listed in Table 6.1:

Table 6.1: Description of application of the model illustrated in Fig. 6.1. Numbering after lifetime estimation indicates the detail level of the simulation. More levels could be defined according to interest and level of information available.

Motivation	**Model**	**Input**
Design analysis	Full scale model. (1) Electro-thermal simulation running until reaching steady cycle. (2) Calculation of degradation parameters for a limited number of cycles.	-Full geometry in CAD format -Load ($i_c, V_{DC}, T_A, T_{cooling}$) -Production description (components, interconnections, process) -Test data *(If available)*
Lifetime estimation (*1) Degradation analysis	Full scale model. (1) Electro-thermal simulation running until reaching steady cycle. (2) Degradation simulation until reaching criteria for fracture propagation. (3) Evaluate physical parameters: forward voltage (V_{ce}, V_F), thermal impedance (Z_{th}), degradation level. Assess necessity for update of electro-thermal simulation. (4) Continue cycle (1)-(3) until reaching failure criteria.	-Full geometry in CAD format -Load ($i_c, V_{DC}, T_A, T_{cooling}$) -Production description (components, interconnections, process) -Test data *(If available)*
Lifetime estimation (*2)	Limited or full scale geometry depending on input. (1) Degradation simulation until reaching criteria for fracture propagation. (2) Continue cycle (1) until reaching failure criteria.	-Geometry of interest -Load ($T(\vec{r},t)$)
Lifetime estimation (*3)	Same procedure as level (*2) but with extrapolation of degradation pattern.	-Geometry of interest -Load ($T(\vec{r},t)$)

CHAPTER 7

Model Theory

7.1 Power Loss

In Sec. 1.1 the standard IGBT power module designs are discussed. Normally, both active (transistors/diodes) and passive elements (interconnections) display losses affecting the module temperature during operation. Power losses in the *Cu* pads, *Al* bond-wires, solders, metallizations, etc. are limited to standard resistive losses. This is not the case with actively switched diodes and IGBTs, here effects like switching-, blocking-, and gate losses also contribute. Based on this the total loss in the semiconductor components far exceed the remaining, meaning the power loss calculation is centred around the semiconductor chips.

The total power loss in a semiconductor component is separated into static (P_{static}), switching (P_s), and driving losses ($P_{driving}$):

$$\begin{aligned} P_{tot} &= P_{static} + P_s + P_{driving}, \\ &\approx P_c + P_s. \end{aligned} \tag{7.1}$$

In Eq. (7.1) P_{static} includes conduction losses (P_c) and blocking losses and as the forward blocking and driving losses are often small compared to the remaining, these are left out.[18, 82, 83]

In devices with an applied on and off current switching between active components the power loss pattern during one switching cycle can be illustrated as in Fig. 7.1. The energy required to turn on (E_{on}), off (E_{off}), and maintain continuous on-state (E_c) heats up the device during active (t_{on}) followed by a passive period (t_{off}).

All parameters are temperature and load dependent meaning:

$$P_{tot} = \frac{1}{T}\int_0^{t_{on}} v_{ce}(t,T)i_c(t,T)dt, \tag{7.2}$$

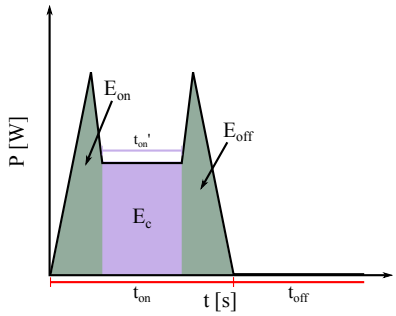


Figure 7.1: Power loss in switched devices.

where $T = t_{on} + t_{off}$. On-state losses are separated into conduction and switching losses as illustrated in Fig. 7.1:[83–85]

$$P_c = \frac{1}{T}\int_0^{t'_{on}} v_{ce}(t,T)i_c(t,T)dt, \tag{7.3}$$

$$P_s = \frac{1}{T}\left(E_{on}(i_c,T) + E_{off}(i_c,T)\right). \tag{7.4}$$

The reason for separation of conduction and switching losses is due to lack of detailed switching characteristics of power semiconductors. Normally, the only supplied information is the switch-loss energy as a function of applied current and to some degree temperature. Formulation of the actual power loss in a given system is therefore highly dependent on the loading and the system response. Detailed discussions on switching characteristics and power loss in dynamic and static systems are available in numerous publications.[82, 84–88]

7.1.1 Power Loss in Three-Phase Converter Simulator

In the test system presented in Sec. 3.1 a well-defined current load is applied under controlled conditions, see Table 3.1. As presented in Eqs. (7.3) and (7.4) the total chip losses are therefore quickly derived from the system modulation function (m):[18, 82]

$$P_c^{IGBT} = i_c(\vec{r},t)v_{CE}(\vec{r},t,T)\left(\frac{1-m}{2}\right), \tag{7.5}$$

$$P_s^{IGBT} = f_s\left[E_{on}(T) + E_{off}(T)\right]\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v^I}, \tag{7.6}$$

$$P_c^{Diode} = i_F(\vec{r},t)v_D(\vec{r},t,T)\left(\frac{1+m}{2}\right), \tag{7.7}$$

$$P_{rec}^{Diode} = f_s\left[E_{rec}(T)\right]\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v^D}. \tag{7.8}$$

The last term $\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v}$ in the switch-loss equations (7.6) and (7.8) are a calibration term as E_{on}, E_{off}, and E_{reg} are normally only specified at one DC-link voltage[18]. V_{ref} is the reference voltage from the datasheet and K_v is the shape correction parameter.

As illustrated in the arguments of the switch losses in Eqs. (7.6) and (7.8) the switching and recovery loss are assumed homogeneously distributed with regard to current but not temperature. Conduction losses are distributed according to current distribution and temperature.

Current Distribution and Passive Element Conduction Loss

Deriviation of the current distribution inside a complex geometry as the one illustrated in Fig. 1.1 is not a trivial task. Especially, when regarding transient conditions all electrical parameters of the individual sections are needed. These are normally not available and can therefore not be applied. Presently, a distribution approach is considered where the current distribution between sections is the initial step, the chip current distribution is the second, and the local wire current the third.

The distribution between sections is most easily handled through a standard circuit analysis[89]. In the present model this is coupled with geometry simplification as will be discussed in a following chapter.

Current distribution on chip and passive elements are derived in steady state in steps through FEM modelling: *(1) Terminal to solder backside, (2) Solder backside through chip and bond wires, (3) bond wires to terminal*. The set of equations are similar to the previously presented convection-reaction-diffusion equation, but with the electric potential instead of the temperature field.

In Fig. 7.2 the relative current in steady state between the ten *Al* wires on the LS IGBT chip is presented. Three different curves are included: a current distribution simulation (i^r_w), a current distribution simulation with temperature effects (i^r_w *T-cal*), and experimental values obtained using four-point probing. Figs. 7.3 illustrate the difference in the current density distribution inside the IGBT chip without (a) and with (b) temperature effects.

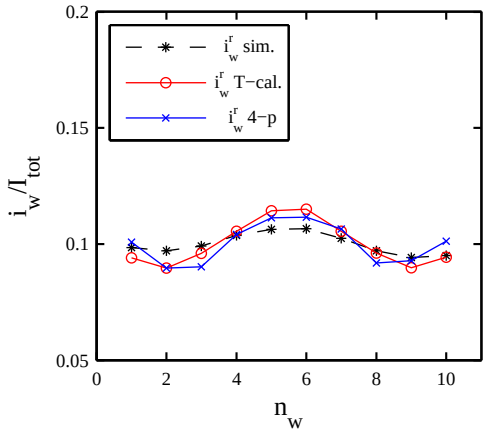
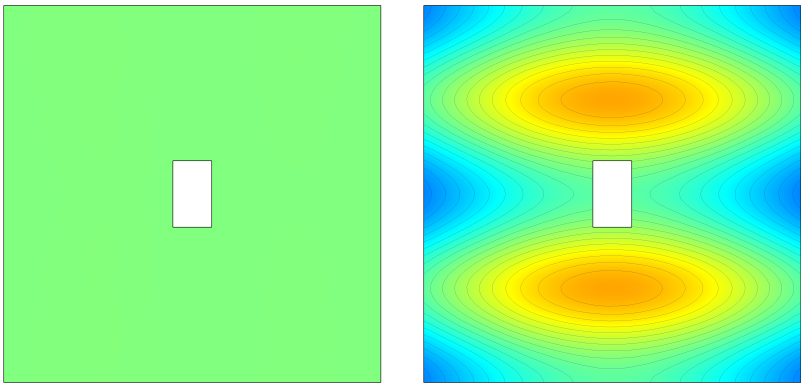


Figure 7.2: Simulated relative wire current of LS IGBT bond wires. Two simulated curves (without and with temperature effects) compared to experimental data.



(a) Current density inside IGBT at constant temperature.

(b) Current density inside IGBT with temperature hotspots.

Figure 7.3: Current density inside LS IGBT chip with even and uneven temperature distribution. The distribution in (b) is induced by a temperature gradient of 25K from hotspots to edge.

Using the steady state relative current distribution the conduction loss may be derived directly from the material conductivity. All pure materials are treated using textbook data, the semiconductor device data are obtained from the power module datasheet. This can be done by direct interpolation or in order to extrapolate outside datasheet specifications by fitting a

model. Presently, a Shockley model is used in series with a resistor:[5, p.107]

$$v_{ce} = n \cdot \frac{k_B T}{q} \cdot \ln\left(\frac{i_c}{I_S} + 1\right) + R \cdot i_c + V_0, \tag{7.9}$$

where n is the carrier concentration, I_S is the saturation current, and V_0 is the offset voltage. The model fitting is carried out for all available datasheet IV curves, meaning a set of input parameters is obtained for each temperature curve. In between and outside provided data, temperature effects are assumed linear.

7.2 Heat Transfer

The study of heat transfer concerns a number of topics, like estimating the flow of energy (in the form of heat) through a system under steady and transient conditions. Naturally, the theory is governed by the laws of thermodynamics, motion, and conservation. The normal approach in heat transfer problems is to use a set of rate equations to analyse the given structure. Transfer of thermal energy into a given control volume is separated into four categories:

- Conduction or diffusion: Tranfer of energy between objects that are in physical contact.
- Convection: Transfer of energy between an object and its environment due to fluid motion.
- Radiation: Transfer of energy to or from a body by means of emission or absorption of electromagnetic radiation.
- Mass transfer: Transfer of energy from one location to another as a side effect of physically moving an object.

The first mentioned is the dominating one in our problematic concerning the heat transfer within a solid medium with no fluid flow. [34, 90, 91]

7.2.1 The Conduction Rate Equation

The conduction rate equation is the same as Fourier's law - the heat rate in the n'th direction is written as:

$$q_n = -k_n A \frac{dT}{dn}, \tag{7.10}$$

where q_n is the rate of power $[W]$, k_n is the thermal conductivity $[Wm^{-1}K^{-1}]$, A is the cross-sectional area of the medium regarded with n being the normal direction to A, and T is the temperature. Often it is more convenient to talk about the heat flux which is defined as

$$q''_n = \frac{q_n}{A} = -k_n \frac{dT}{dn}. \tag{7.11}$$

Eq. (7.11) is only valid if A is an isothermal surface[34, p. 59]. From Eq. (7.11) the generalized heat flux equation becomes:

$$\vec{q}'' = -\boldsymbol{k}\vec{\nabla}T(\vec{r},t), \tag{7.12}$$

where $\vec{\nabla}$ is the del operator. And the derivatives in Eqs. (7.10) and (7.11) are replaced with partial derivatives. From (7.12) it is clear

$$q''_x = -k_x \frac{\partial T}{\partial x}, \qquad q''_y = -k_y \frac{\partial T}{\partial y}, \qquad q''_z = -k_z \frac{\partial T}{\partial z}. \tag{7.13}$$

The equations in Eq. (7.13) relates the heat flux across a surface to the temperature gradient in a direction perpendicular to the surface.[34, 91]

7.2.2 The Heat Diffusion Equation

Generally one often wish to determine the temperature field (or distribution) inside a medium resulting from conditions imposed on the boundaries. For a solid, knowledge of the temperature distribution makes it possible to determine the structural integrity through thermal stresses, expansions, and deflections.

Deriving the set of equations from which the temperature field may be obtained is carried out through a set of steps: *(1) introduce a differential control volume, (2) identify relevant energy transfer processes,* and *(3) introduce rate equations*. These steps should yield a differential equation from where (for certain boundary conditions) the temperature field may be derived.[34, 91]

In Fig. 7.4 a control volume is depicted:

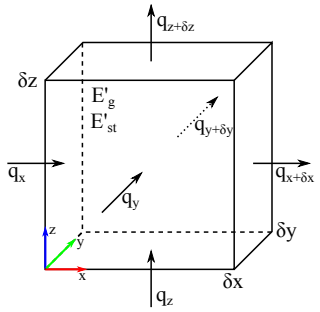


Figure 7.4: Heat flux through an infinitesimal cube. Inspired from [34, p. 70].

If a temperature gradient exist inside the medium a conduction of heat occurs across the control surface. The heat rates perpendicular to the faces of the cube is denoted q_x, q_y, and q_z, according to the specified coordinate system. Conduction heat rates at the opposite faces are expressed using a Taylor series expansion (neglecting higher order terms):

$$q_{x+\delta x} = q_x + \frac{\partial q_x}{\partial x}\delta x, \tag{7.14}$$

and similar for y and z[*1].

Within the medium there may be an energy source term associated with the rate of thermal energy generated[*2]:

$$\frac{\partial E_g}{\partial t} = \frac{\partial q}{\partial t}\delta x\delta y\delta z \tag{7.15}$$

where E_g is the generated thermal energy, q is the rate of generated thermal energy, and $\delta x\delta y\delta z = V_{DCV}$ is the volume of the differential control volume. If the material is not experiencing a change in phase, the energy storage term may be expressed as:

$$\frac{\partial E_{st}}{\partial t} = \rho c_p \frac{\partial T}{\partial t} V_{DCV}, \tag{7.16}$$

where ρ is the material density and c_p is the specific heat capacity at constant pressure. Based on energy contributions and rate equations the energy conservation requires:

$$\frac{\partial E_{in}}{\partial t} + \frac{\partial E_g}{\partial t} - \frac{\partial E_{out}}{\partial t} = \frac{\partial E_{st}}{\partial t}. \tag{7.17}$$

It is clear that E_{in}/E_{out} in our example depends on the conduction heat rates, thus:

$$q_x + q_y + q_z + \frac{\partial q}{\partial t}V_{DCV} - q_{x+\delta x} - q_{y+\delta y} - q_{z+\delta z} = \rho c_p \frac{\partial T}{\partial t} V_{DCV}, \tag{7.18}$$

$$q_x + q_y + q_z + \frac{\partial q}{\partial t}V_{DCV} - q_x - \frac{\partial q_x}{\partial x}\delta x - q_y - \frac{\partial q_y}{\partial y}\delta y - q_z - \frac{\partial q_z}{\partial z}\delta z = \rho c_p \frac{\partial T}{\partial t} V_{DCV}, \tag{7.19}$$

$$\frac{\partial q}{\partial t}V_{DCV} - \frac{\partial q_x}{\partial x}\delta x - \frac{\partial q_y}{\partial y}\delta y - \frac{\partial q_z}{\partial z}\delta z = \rho c_p \frac{\partial T}{\partial t} V_{DCV}. \tag{7.20}$$

We insert Fourier's law, see Eq. (7.10), and divide away the volume of the differential control element[*3]:

$$\frac{\partial q}{\partial t} + \frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) = \rho c_p \frac{\partial T}{\partial t}. \tag{7.21}$$

[*1] This is given as the heat rate at $x+\delta x$ can be written as the rate at x plus the gradual change $\frac{\partial q_x}{\partial x}$ times the distance dx.

[*2] Eg. through work performed inside the cube - ohmic loss, switch loss, etc.

[*3] $\frac{\partial}{\partial n} q_n \delta n = -\frac{\partial}{\partial n}\left(k_n A \frac{\partial T}{\partial n}\right)\delta n = -\frac{\partial}{\partial n}\left(k_n \frac{\partial T}{\partial n}\right) V_{DCV}$

Eq. (7.21) is the generalized heat diffusion equation in Cartesian coordinates. The solution is the temperature field $T(\vec{r},t)$. If we express Eq. (7.21) in terms of the $\vec{\nabla}$ operator:

$$\frac{\partial}{\partial t}q(\vec{r},t)+\vec{\nabla}\cdot\left(k\vec{\nabla}T(\vec{r},t)\right)=\rho c_p\frac{\partial}{\partial t}T(\vec{r},t) \tag{7.22}$$

In Eq. (7.22) the first term on the left describes the change in storage of internal energy within the body, the second term is the steady-state heat transfer term, and the term on the right describes the transient properties of the temperature. This equation is basically a diffusion-convection-reaction equation and is ideal for a finite element approach, this is presented in a following section[92].

7.2.3 Convection

In the previous section the concept of conduction is presented. Here it was briefly mentioned that at the boundary between a solid and a liquid heat is transferred via convection instead of conduction. This may in many cases be handled simply as a boundary condition (BC), but the coefficients used in the BC must be specified. Convection includes the transfer of energy by bulk fluid motion (advection) and random movement of molecules (diffusion). The subject of convection may be complicated depending on the nature of it. One may experience phase changes or irregular motion of one of the components in the situation. For now we merely look at the boundary situation relevant for water cooling of a given component.[93, 94]

Boundary Layer

When a fluid is in contact with a surface the nearest particles' velocity is decreased to zero by the interacting forces. The nearest particles then affect the next nearest an so on resulting in a reduced flow near the surface. This is illustrated in Fig. 7.5.

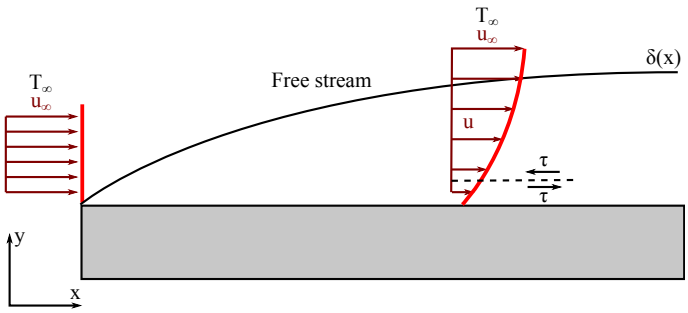


Figure 7.5: Illustration of the loss of flow velocity in a fluid near a surface, the arrows indicate the flow speed. Inspired from [34, p. 349].

The impact on flow velocity is due to shear stresses τ acting parallel to the surface and the direction of the fluid velocity. Naturally this effect decreases with the distance y from the surface until the maximum velocity u_∞ is reached. We define this distance as δ which is normally referred to as the boundary layer thickness. Accordingly, two regions outside the solid exists, a layer with a varying flow velocity/temperature and a stationary layer. The effect of shear stresses is often described through a friction coefficient:

$$C_f = \frac{\tau_s}{\frac{1}{2}\rho u_\infty^2}, \qquad \tau_s = \mu \frac{\partial u}{\partial y} \tag{7.23}$$

where μ is the dynamic viscosity. The definition of the surface shear stress in Eq. (7.23) only holds for Newtonian fluids. [34]

The thermal effects in a fluid passing a solid surface are directly related to the velocity of the liquid. Before the liquid reaches the surface the temperature is uniformly distributed and constant T_∞. After reaching the surface the nearest particles will, in the same manner as the velocity case, feel the most significant affect. This is illustrated in figure 7.6 where we assume $T_s > T_\infty$.

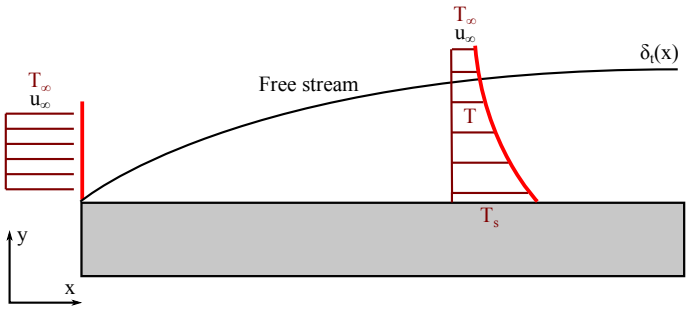


Figure 7.6: Illustration of the transfer of heat into a fluid near a surface where $T_s > T_\infty$, the maroon lines indicate the local temperature by length. Insprired from [34, p. 350].

Again δ_t is the distance from the surface where the stationary liquid temperature is nearly reached:

$$\delta_t = \frac{T_s - T}{T_s - T_\infty} \tag{7.24}$$

Now the heat flux into the liquid may be derived by applying Fourier's law in $y = 0$:

$$q_s'' = -k_f \left.\frac{\partial T}{\partial y}\right|_{y=0} \tag{7.25}$$

Eq. (7.25) holds true because of the situation explained in the previous section. The fluid velocity is zero, therefore all energy transfer is through conduction. By combining Eq. (7.25)

with Newton's law of cooling, see [94][*4], one has:

$$h = \frac{-k_f}{T_s - T_\infty} \left.\frac{\partial T}{\partial y}\right|_{y=0}. \tag{7.26}$$

As would be expected the shape of the temperature curve away from the surface increases with x until a given stationary situation is reached[*5]. Eq. (7.26) reduces the boundary convection problem into determining the convection parameter h. This is, however, a complicated problem which is normally solved by estimating an effective value either through FEM simulation or experimental values.[66, 95]

7.3 Structural Mechanics

Structural mechanical analysis of an arbitrary solid subjected to a given mechanical loading is by no means a trivial task. Several approximations are used in real life chosen based on type of solid, application, and purpose of analysis. Mechanical loading of structures will over time result in what is defined as flow, which, in principle, are processes occurring on atomic level due to the change state. Accordingly, the detail of a complete mechanical analysis often exceed what is possible[96–98].

Numerous approximations exist all depending on the level of detail included. The simplest form is to regard reversible processes independent of time and space (elastic regime). This is often expanded to include small irreversible contributions making it dependent on space (elasto-plastic regime). Further improvement of the model is often a complicated process making it necessary to use approximations to implement rate- [99] or temperature dependency [97], viscosity [52], etc. The presently discussed theory is centred on obtaining the stress (σ) and strain (ε) as a function of position and time. Therefore, the central aspect is the stress-strain curve:[100–102]

The separation of an elastic an plastic regime makes it necessary to distinguish between the regimes depending on loading as well as response.

7.3.1 Linear Elasticity

In the linear elastic case all processes are fully reversible and therefore it is only necessary to look at the stationary example. Initially we regard an arbitrary solid structure subjected to external loads:

[*4] $q_s'' = h(T_s - T_\infty)$

[*5] The applied theory is based on gradient induced fluxes, accordingly, exact same situation as the velocity and thermal boundary layer may be derived with regards to mass transfer, see [34]

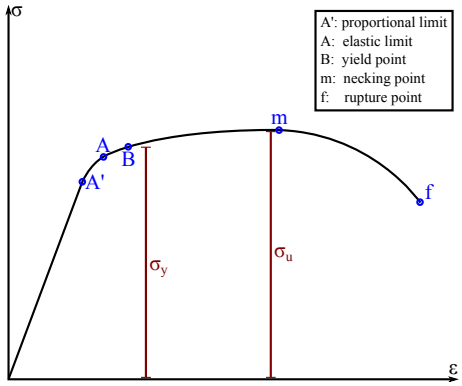


Figure 7.7: Stress-strain curve illustration with emphasis on relevant points. σ_y is the material yield strength, and σ_u is the ultimate tensile strength

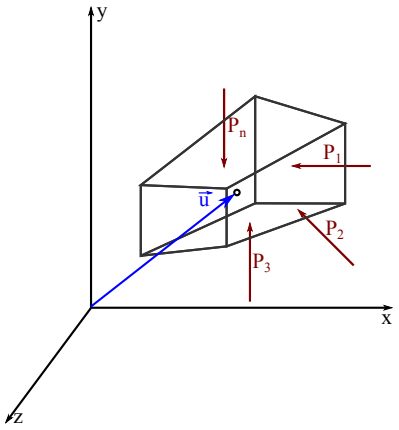


Figure 7.8: An external pressure is applied on an arbitrary solid structure resulting in deformation and internal resistance.

The applied load induce in two reactions - deformation followed by internal resistance. Accordingly, a new material equilibrium is reached but with internal resistance everywhere. The common approach is to describe this through the so-called stress vector[100, 103, 104].

Around position $\vec{u}$ we regard a differential element of area ΔA where a force (ΔF) is experienced in an arbitrary direction. The stress vector in the normal and tangential direction

of the differential element is thus

$$\vec{t}_n = \lim_{\Delta A \to 0} \frac{\Delta \vec{F}_n}{\Delta A}, \tag{7.27}$$

$$\vec{t}_t = \lim_{\Delta A \to 0} \frac{\Delta \vec{F}_t}{\Delta A}. \tag{7.28}$$

These are defined as the normal ($\vec{\sigma}_n$) and shear stress ($\vec{\sigma}_t$)[*6]. By orientating them with respect to a Cartesian coordinate system a full stress matrix may be defined:

$$\boldsymbol{\sigma} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix} \tag{7.29}$$

It follows that $\sigma_{xy} = \sigma_{yx}$ due to symmetry, and thus the matrix, $\boldsymbol{\sigma}$, may be reduced to a row vector:

$$\vec{\sigma} = \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{yz} \\ \sigma_{xz} \end{bmatrix} \tag{7.30}$$

The applied stress cause displacements as a function of the amplitude. This means that the position of a point is altered. We refer to the relative change as the local strain ($\boldsymbol{\varepsilon}$) and derive the different strain components from the position alteration compared to a normal and tangential direction:

$$\vec{\varepsilon} = \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{yz} \\ \varepsilon_{xz} \end{bmatrix} = \begin{bmatrix} \frac{\partial}{\partial x} & 0 & 0 \\ 0 & \frac{\partial}{\partial y} & 0 \\ 0 & 0 & \frac{\partial}{\partial z} \\ \frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \\ 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} & 0 & \frac{\partial}{\partial x} \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{7.31}$$

Derivation of the strain field from an applied stress is even for linear elastic materials often a complicated problem, at-least with respect to computational demands. In general the situation is regarded by solving the constitutive equation:

$$\vec{\sigma} = \boldsymbol{C} \cdot \vec{\varepsilon}, \tag{7.32}$$

[*6]Often it is customary to regard to types of strain - engineering (Eulerian) and true (Lagrangian). The former only takes initial and final shape of the solid into account, and the latter is at all times dependent on present state. In the present work all strain is regarded as true strain except in the pure elastic regime.[100]

where $\boldsymbol{C}$ is a six times six tensor, which is clear from Eqs. (7.30) and (7.31). The actual derivation of elastic constants of $\boldsymbol{C}$ depends on geometry, approximations, flow, BCs, etc.[104]

Generalized Hooke's Law

In isotropic solids in equilibrium a unique relation exist between the stress and strain components:

$$\sigma_{ij} = \sum_{k=1}^{3} \lambda \varepsilon_{kk} \delta_{ij} + 2G\varepsilon_{ij}, \tag{7.33}$$

where G is the shear modulus of elasticity, δ is the Kronecker delta, and λ is the Lame constant:

$$\lambda = \frac{E\nu}{(1+\nu)(1-2\nu)}$$

where E is the modulus of elasticity and ν is the Poisson's ratio. Several other constitutive relations may be derived by simplifying Eq. (7.33) further, however, the present shape is the general case for isotropic linear elastic solids.[100, 104]

Effective Stress and Strain

From Eqs. (7.30) and (7.31) it is evident that a material under stress may have up to six independent stress and strain components. It is often desired to have a general idea of the combined load experienced, here the so-called effective stress and strains are introduced:

$$\overline{\sigma} = \frac{1}{\sqrt{2}} \left[(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_x - \sigma_z)^2 + 6(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{xz}^2) \right]^{1/2} \tag{7.34}$$

$$\overline{\varepsilon} = \frac{\sqrt{2}}{3} \left[(\varepsilon_x - \varepsilon_y)^2 + (\varepsilon_y - \varepsilon_z)^2 + (\varepsilon_x - \varepsilon_z)^2 + 6(\varepsilon_{xy}^2 + \varepsilon_{yz}^2 + \varepsilon_{xz}^2) \right]^{1/2} \tag{7.35}$$

The effective stress is often referred to as the Von Mises stress when the Von Mises yield criterion[*7] is being used.[100, 101]

7.3.2 Plasticity and Flow

In the present work the concept of rate-independent plasticity is utilized to formulate constitutive relations. In principle this is based on infinitesimal deformation, but has been shown to be valid for finite deformation as well.[60, 101, 105]

[*7] Large amount of material parameters are used when dealing with stress/strain relations, however, ordinarily only tensile test data is available. Information regarding the yield limit (σ_y) is overcome through the Von Mises yield criteria simply by assuming: $\overline{\sigma} = \sigma_y$.

Initially the strain rate is decomposed into the elastic and plastic contribution:

$$\dot{\varepsilon}_{ij} = \dot{\varepsilon}_{ij}^{(e)} + \dot{\varepsilon}_{ij}^{(p)} \tag{7.36}$$

where the first term on the right hand side is a fully reversible elastic strain, and the latter is the non-reversible plastic contribution. The decomposition is illustrated in Fig. 7.9, where in this particular case $\varepsilon^{(e)} = \varepsilon_2 - \varepsilon_1$ and $\varepsilon^{(p)} = \varepsilon_1$.

The elastic strain rate is solved directly from the theory introduced in the previous section. The inelastic contribution is obtained through the plastic potential function $F(\vec{\sigma})$:

$$\frac{d\varepsilon_p}{dt} = \frac{d\lambda}{dt}\frac{\partial F(\vec{\sigma})}{\partial \sigma}, \tag{7.37}$$

where λ is the plastic multiplier and $F(\vec{\sigma})$ for a Von Mises type isotropic strain-hardening material is

$$F(\vec{\sigma}) = \sigma_{VM}(\vec{r}) - \sigma_y(\vec{r}), \tag{7.38}$$

where σ_{VM} is the Von Mises stress, and σ_y is the yield strength.

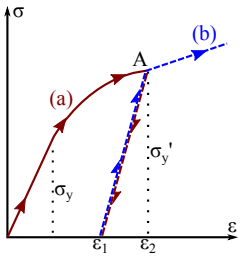


Figure 7.9: Loading beyond elastic limit, unloading (a), and reloading (b) paths of solid with plastic deformation.

Flow Curves

Analytically, one normally looks at three cases of plastic material behaviour: (a) rigid ideal plastic deformation, (b) ideal elasto-plastic deformation, and (c) elasto-plastic deformation with hardening, see Fig. 7.10. Additional approximated models are being used e.g. the one developed by Richard and Blacklock[106]:

$$\sigma = E\varepsilon\left[1 + \left(\frac{E\varepsilon}{(1 - E'/E)\sigma_k + E'\varepsilon}\right)^n\right]^{-1/n}, \tag{7.39}$$

where σ_k is at A in Fig. 7.7 and n is a shape parameter $n \approx \ln(2)/\ln(\sigma_k/\sigma_0)$ with σ_0 being the linear shape limit. Such models always work with success depending on regarded material. In reality type (c) from figure 7.10 should always be used. And it should even be modified with a gradual changing hardening as in (d).

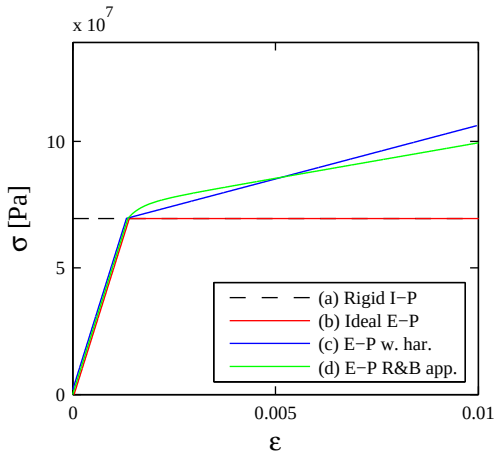


Figure 7.10: Elasto-plastic flow curves for analytical handling of plastic problems. (a) rigid ideal plastic deformation, (b) ideal elastic-plastic deformation, (c) elastic-plastic deformation with hardening, and (d) Richard and Blacklock elasto-plastic approximation see Eq. (7.39).

7.3.3 Thermal Stress

If the temperature of a body changes by ΔT the body experiences a uniform strain. If ΔT is positive the body expands and vice versa when ΔT is negative. The change in length may be written as:

$$\Delta L_i = L_i \alpha \Delta T \quad , i = x, y, z \tag{7.40}$$

If the body is homogeneous then the strain may be written as:

$$\vec{\varepsilon}_{th} = \alpha_{xyz} \cdot [1\ 1\ 1\ 0\ 0\ 0]^T \Delta T, \tag{7.41}$$

where α_{xyz} is the CTE tensor which reduces to α for linear isotropic materials [104, Ch.7]. Following this equation the strain and thus the displacement field due to a temperature change may be evaluated directly from the temperature field[104, 107].

Thermal Strain Approximation

Ideally the thermal stress should be evaluated from the approach discussed in the previous section. However, a simplified analytical approach is sometimes preferable. This approximation presents a short method to calculate the thermo-mechanical stress. In Fig. 7.11 a 1D

illustration of the stress created between to layers is presented.

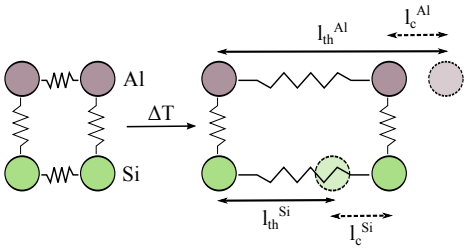


Figure 7.11: Illustration of a 2 layer approximation of the thermal expansion of an *Si*/*Al* interface.[8, 43].

Directly in the interface one would observe a connection between *Al* and *Si*. If isolated from each other the materials would expand according to the expansion coefficient α^i. When placed in connection the mismatch in CTE creates a constraint on both layers (l_c^i). As illustrated in Fig. 7.11 the expansion of *Al* is limited by *Si* and vice versa for the expansion of *Si*. *Si* behaves in a brittle manner, accordingly it only experiences an elastic deformation ($\varepsilon^{Si} = \varepsilon_{el}^{Si}$), whereas the ductile manner of *Al* has the possibility of both elastic and plastic deformation($\varepsilon^{Al} = \varepsilon_{el}^{Al} + \varepsilon_{pl}^{Al}$). If one assumes the total strain is the same in *Al* and *Si* it follows

$$\varepsilon_{th}^{Al} - \varepsilon_{el}^{Al} - \varepsilon_{pl}^{Al} = \varepsilon_{th}^{Si} + \varepsilon_{el}^{Si} \tag{7.42}$$

$$\varepsilon_{pl}^{Al} = \varepsilon_{th}^{Al} - \varepsilon_{el}^{Al} - \varepsilon_{th}^{Si} - \varepsilon_{el}^{Si} \tag{7.43}$$

$$= \left(\alpha^{Al} - \alpha^{Si}\right)\Delta T - \left(\frac{\sigma_y^{Al}}{E^{Si}} + \frac{\sigma_y^{Al}}{E^{Al}}\right) \tag{7.44}$$

2D Plane Strain Approximation

The thermal stress is primarily orientated in the plane of the interface of the two materials and accordingly the tensile strain in the plane is, in the elastic regime, easily derived from the thermal stress. However, in the direction normal to the interface plane the strain is a bit more difficult to calculate analytically. By looking at the interface between two materials, see Figure 7.12, exposed to a planar stress an approximation may be derived from the principal of volume conservation.

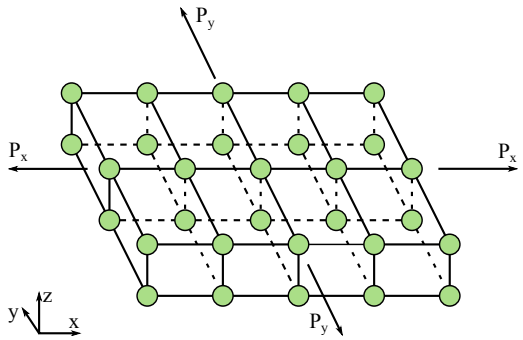


Figure 7.12: Illustration of a 2D structure experiencing a homogeneous pressure in the x and y direction. The resulting expansion is likewise uniform and homogeneous.

If the two layers have a mismatch in CTE one of the layers experiences a force acting towards natural thermal expansion and vice versa for the other material. This is specified in a Sec. 7.3.3. For now, an infinite layer is subjected to a constant uniform stress in the x and y direction called P_x and P_y, see Fig. 7.12. The volume before applying the stress is defined as

$$V_1 = x_1 y_1 z_1$$

After applying the pressure the material is expanded and the resulting volume is

$$V_2 = x_2 y_2 z_2 = (x_1 + \Delta x)(y_1 + \Delta y)(z_1 + \Delta z)$$

If volume conservation ($V_1 = V_2$) is required[*8] one has

$$\begin{aligned} x_1 y_1 z_1 &= (x_1 + \Delta x)(y_1 + \Delta y)(z_1 + \Delta z) \\ &= x_1 y_1 z_1 + x_1 y_1 \Delta z + x_1 z_1 \Delta y + x_1 \Delta y \Delta z + y_1 z_1 \Delta x + y_1 \Delta x \Delta z + z_1 \Delta x \Delta y + \Delta x \Delta y \Delta z \end{aligned}$$

Dividing by the initial volume and utilize the definition of tensile strain one has

$$\begin{aligned} 0 &= \varepsilon_z + \varepsilon_y + \varepsilon_y \varepsilon_z + \varepsilon_x + \varepsilon_x \varepsilon_z + \varepsilon_x \varepsilon_y + \varepsilon_x \varepsilon_y \varepsilon_z, \\ &\Downarrow \\ \varepsilon_z &= -\frac{\varepsilon_y + \varepsilon_y \varepsilon_x + \varepsilon_x}{\varepsilon_y + \varepsilon_y \varepsilon_x + \varepsilon_x + 1}, \end{aligned}$$

where the minus sign indicates that if the material is expanded in the x and y direction the material has to be contracted in the z direction to keep the volume constant. In the case of an isotropic medium with the same pressure applied $\varepsilon_y = \varepsilon_x = \varepsilon_{plane}$:

$$\varepsilon_z = -\frac{\varepsilon_{plane}^2 + 2\varepsilon_{plane}}{\varepsilon_{plane}^2 + 2\varepsilon_{plane} + 1} \tag{7.45}$$

[*8] Natural expansion of the layer with the lowest CTE has to be subtracted from V_2

With thermal expansion the strain is often small and accordingly a Taylor series is used for the relation, Eq. (7.45), between in-plane stress and out-of-plane stress:

$$\varepsilon_z = -2\varepsilon_{plane}. \tag{7.46}$$

Eq. (7.46) is naturally an approximation. The geometry for instance is not taken into account. If the interface is not perfectly planar and homogeneous like in Fig. 7.12 the thermal stress vector also has components in the z-direction. This also has impact on the isotropic assumption. Finally in reality the thermal strain may be so high that the Taylor expansion no longer holds.

7.4 Fracture Mechanics

In part I the bond wire lift-off failure process was introduced with comments that the fracture path was often observed to move in a vertical direction inside the wire itself, with respect to chip surface, to a given height. The reason for this is that over time, when subjected to cyclic stress, cracks are initiated around voids, interface termination regions, etc. or what might be referred to as natural sites. Due to the strength of crystalline grains compared to inter-grain bonds, cracks may propagate at grain boundaries[43]. As presented in Sec. 5.3.1 the wire bonding process often refines the grains near the interface, meaning the average grain diameter increases when moving inside the wire itself. When the grain diameter increases the yield strength decreases which is referred to as the Hall-Petch relation:

$$\sigma_y = \sigma_0 = +k_y d^{-1/2} \tag{7.47}$$

where σ_y is the yield strength, k_y is the dislocation locking term, d is the grain diameter, and σ_0 is the yield strength for dislocation along slip planes[79, 108]. The change in yield strength due to the micro-structure explains the reason for bond wire lift-off cracks to often move inside wires themselves. Similarly, other material degradation processes are related to the microscopical structure and atomic scale processes.[97]

7.4.1 Material Damage

For simplicity the types of damage observed in solids are divided into different groupings, see Table 7.1, in common, is its creation by initiation of surfaces. This may be through cracks, voids, etc. and at different scales but in general it is linked with microscopic processes. Three fundamental types are regarded on the atomic scale: *(a) cleavage, (b) slip with step formation,* and *(c) creation of cavities*, see Fig. 7.13.[96, 98]

The assignment is to link the microscopic damage to macroscopic processes. Doing this requires considering crack initiation, crack mechanisms and path (phases, constraints), and load conditions (including environment). These are in principle interconnected at may vary over time.

Table 7.1: Grouping of damage processes in solid materials, inspired from [98].

	Volume damage	**Surface damage**
Abrupt	Cleavage	Liquid metal embrittlement
	Cavities (Trans- or intergranular)	
Time dependent	Creep	Fatigue
	Irradiation embrittlement	Wear
	Impurity embrittlement	Stress corrosion
	Hydrogen embrittlement	Corrosion fatigue

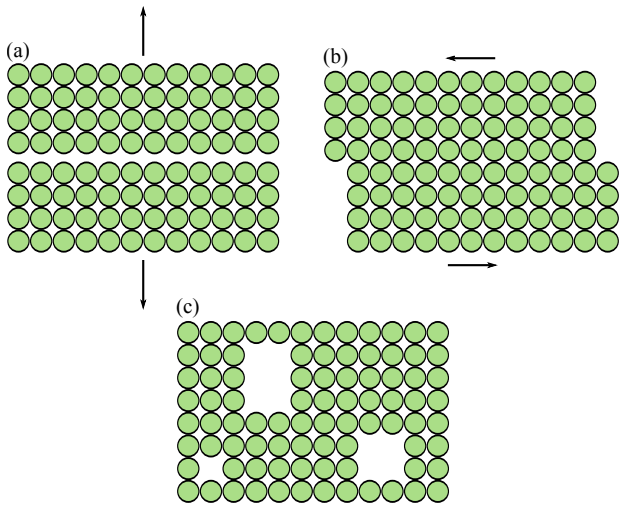


Figure 7.13: Schematic of atomic scale damage processes, (a) cleavage, (b) slip, and (c) creation of cavities - inspired from [98].

7.4.2 Fatigue Crack Growth

Under cyclic loading a given structure, naturally, deforms according to the load as described in Sec. 7.3. If only reversible elastic deformation occurs the concept of fatigue damage cannot occur. Accordingly, reversible yield limits needs to be exceeded to create permanent damage. In crystalline solids the irreversibility is created by dislocations which lead to slips. The reason for initiation near the surface, as presented in Table 7.1, is less constraint on the free side rendering the slip process easier. Normally, fatigue processes are separated into long and short crack processes[109] which are related to the loading. We will limit ourselves to the latter due to the stress normally experienced in power modules, which goes under so-called low cycled fatigue, but for additional detail refer to [96, 110].[111]

Short cracks are initiated from slips at the surface and grow in grain planes until reaching a grain boundary at a specific angle resulting in slowing down propagation. Further propagation is limited by the considered geometry. Normal condition would be to continue intergranular movement at a slightly different angle. The flow rate is expected to be proportional to grain size as described by the Hall-Petch relation, but depending on the grain dislocations this is not definitive[110, p.330]. Doing calculation on this type of fracture is closely controlled by the strength of the component. Macroscopically this is put into a single parameter - the fatigue strength. Number of cycles to fracture (N_R) was proposed by Coffin and Manson independently to relate to the cyclic strain amplitude through the famous Coffin-Manson relation:[111]

$$N_R = A' {\Delta\varepsilon_p}^{-\alpha'} \tag{7.48}$$

where α', A' are experimentally determined parameters and $\Delta\varepsilon_p$ is the plastic strain amplitude. The relation is only valid in the medium strain regime within the low cycle fatigue range. Formulation of the relation is based on the strain decomposition approximation defined in Sec. 7.3.2.

Conceptually, the Coffin-Manson relation can be explained by regarding the fatigue process from micro- to macro-scale. In micro-regime the rupturing is initiated by the before mentioned dislocation movement or slips. After approximately 10% lifetime the microscopic rupturing changes into mesocracks or cracks on the mesoscopic scale. It has been stated that the appearance of mesocracks can be regarded as a stochastic process with nucleations in random positions at the surface, according to geometry[111]. Depending on loading the mesocracks will over time begin forming clusters which are grouped by type and phase (intergranular, transgranular, etc.). Bulking of mesocracks also enable the final stage of the low cycle fatigue. When reaching a critical size the mesoscopic scale damage change into a macroscopic rupture by propagation of the most critical crack through the bulk of the solid. Under these steps the final crack propagation is naturally the main force in the rupture but the main controller is the initiation process between micro- and mesoscopic processes.

7.4.3 Degradation Modelling

Through the model presented in Fig. 6.1 with a full power loss model, temperature field, and strain distribution defined in Secs. 7.1, 7.2, and 7.3, respectively, as input all relevant stressors of a power module are known. However, as discussed in Sec. 7.4.2 the low-cycle fatigue process is very geometry and material dependent. Accordingly, defining a governing lifetime law for a power module consisting of any sub-element and assembled using an arbitrary technique is impossible. Instead, general material degradation (D) is sought derived for estimation of relative damage by a given loading. Actual derivation of absolute values like changes in forward voltage, crack length, etc. would be obtained by comparison to experimental data.

The primary failure mechanism experienced in the module regarded in Secs. 4.3.2 and 5.3.2 placed under the conditions shown in Table 3.1 are identified as bond wire lift-off and metallization reconstruction, see paper G. In [16, 17] a 1D approach for modelling the bond wire lift-off failure mechanisms is presented. It is a time-domain based approach with the primary stressors as input. Fracture propagation criteria are obtained by comparison with shear tests. The model is separated into a damage creation and recovery part:

$$\begin{aligned}\delta D &= f(D,\varepsilon,T)\delta T - \rho(D,T)\delta t \\ &= f_\varepsilon f_D f_T \delta T - \rho_D \rho_T \delta t.\end{aligned} \tag{7.49}$$

In the following section the theory is expanded to 3D and the inputs are time resolved FEM simulations. The main function $D(\vec{r},t)$ of the differential equation in Eq. (7.49) is still a unitless degradation parameter. Any physical interpretation of the absolute value of $D(\vec{r},t)$ has to be obtained by comparing to specified criteria, e.g. fracture propagation by comparison to experimental data or design quality by comparison to damage generated at other positions.

Damage functions

The first term on the right hand side of Eq. (7.49) is the damage generated at time t. As indicated in the equation this is separated into four contributions: Strain concentration function $f_\varepsilon(\vec{r},t)$, hardening function $f_D(\vec{r},t)$, thermal load $f_T(\vec{r},t)$, and a local displacement strain $d\varepsilon_d$:

$$f_\varepsilon(\vec{r},t) = G_0 \varepsilon_p^e(\vec{r},t), \tag{7.50}$$

$$f_D(\vec{r},t) = 1 + a_H D(\vec{r},t)^{B_H}, \tag{7.51}$$

$$f_T(\vec{r},t) = \left(\frac{T_{eq}}{T(\vec{r},t)}\right)^{B_T}, \tag{7.52}$$

$$d\varepsilon_d = \Delta\alpha\delta T, \tag{7.53}$$

where G_0, a_H, B_H, and B_T are computational coefficients and ε_p^e is the effective plastic strain.

Restoration functions

The second term on the right hand side of Eq. (7.49) is the recovery part. ρ_D is the already existing damage and $\rho_T \delta t$ is a temperature activated annealing term depending on the amount of time at the given temperature and the strain hardening experienced prior.

$$\rho_T(\vec{r},t) = \kappa_2 \exp\left(-\frac{E_A}{k_B T(\vec{r},t)}\right), \tag{7.54}$$

where E_A is the activation energy and κ_2 is a computational coefficient.

CHAPTER 8

Degradation in High Power IGBT Modules

In order to derive the thermo-mechanical induced stress and material damage created under a given loading all steps of Fig. 6.1 must be handled. This is done by simulating the dynamic temperature field created by the power loss under operation followed by a calculation of the stress response. From the induced stress the degradation parameter may be obtained for design analysis, damage assessment, or lifetime estimation.

8.1 Dynamic Temperature Field Analysis of IGBT Module

In order to derive the thermo-mechanical induced stress across all interfaces of a full power module, the temperature field needs to be obtained. The regarded geometry is presented in Fig. 1.1 and the load conditions in Table 3.1.

8.1.1 Module Geometry and Material Properties

Calculation of the temperature field around a complex geometry with multiple materials is a complicated matter with regard to theory and computational power. Solving Eq. (7.22) through a FEM approach requires a specified geometry and relevant physical parameters.

Electrical properties of the regarded power module is extracted directly from the component data-sheet, and physical properties of pure materials are textbook listed[34, 97, 112–114]. Whereas other materials like doped silicon[115], ceramics[116, 117], solders[118], etc. are obtained from articles or databases[119]. Handling the complex semiconductor structures is carried out using an effective medium approximation (EMA) which is described in detail in a following section.

Simplified Module Geometry

In Figs. 1.1 and 8.1 a photography and computer aided design (CAD) image of a full IGBT power module is displayed. The CAD image is simplified by leaving out bond wires and terminal pads. Doing a full scale simulation of the temperature field under the load specified in Sec. 7.1.1 is demanding with regard to computational power. Taking electro-thermal coupling as well as the difference in sub-element scale[*1] into account further increase the

[*1] $8.4mm \times 10.6mm \times 6\mu m \approx 0.5mm^3$ *Al* diode metallization vs. $250mm \times 67mm \times 3mm \approx 5e4mm^3$ *Cu* baseplate.

demands.

The initial simplification in the present model is to utilize the periodicity of the six struc-

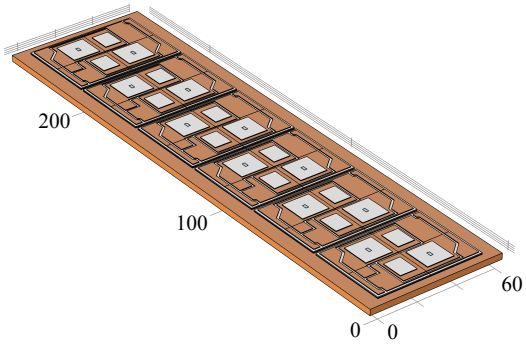


Figure 8.1: CAD illustration of a IGBT power module - from paper F.

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tural identical sections in order to only regard a single section. In Fig. 8.2 a CAD illustration of a single sectioning with all relevant components included and the part of baseplate in its proximity is presented.

Section position on top of the baseplate, however, have been reported on several

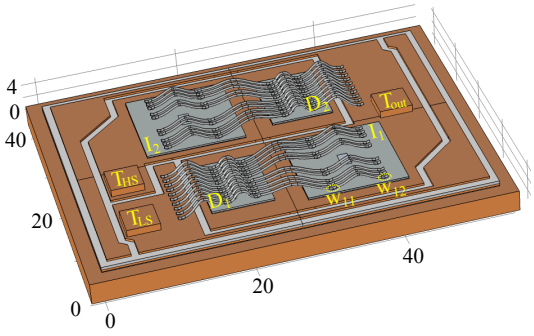


Figure 8.2: CAD illustration of a IGBT power module section - from paper F.

occasions[66, 120] to affect the mean section temperature due to possible heating of cooling reservoir while passing the sample. This is overcome by modulating the effective backside cooling temperature of the regarded section according to position:

$$q''_{SP} = h_{SP}\left[(T_s(x,y,t) + T_{cor}(x,y,t)) - T_{SP}\right], \tag{8.1}$$

where h_{SP} is the convection coefficient at the specific flow rate, T_s is the local surface temperature from the section simulation, T_{SP} is the cooling liquid temperature, and T_{cor} is the

section position correction.

An example of a simplified full module simulation is presented in Fig. 8.3 at an arbitrary time under the conditions specified in Table 3.1. In Fig. 8.4 the baseplate backside and topside temperature is plotted along a line at the module centre with the different section positions marked. Under the cooling conditions applied in the three-phase wind power converter simulator effects from section position is almost limited to S1 and S6.

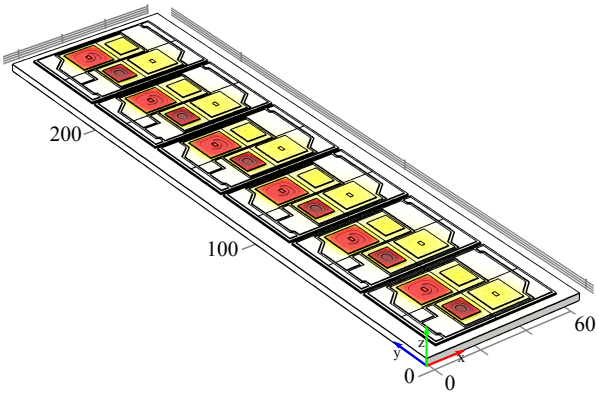


Figure 8.3: Temperature field of simplified full power module subjected to sinusoidal load conditions.

Thermal Conductivity - Effective Medium Approximation

As mentioned in the introduction silicon chips are a complex architecture with different regions. This affects the effective physical parameters (conductivity, expansion, etc.) of the silicon chips. Therefore, either the specific geometry needs to be included in the full scale simulations or an effective approximation can be introduced. The former is problematic as individual layers in IGBT chips have heights as low as a single micron. Compared with e.g. the wire- or the ceramic thickness's this presents a dimensional problem with regard to computational power. Instead symmetry of the semiconductor chips is utilized to regard a single current channel and develop effective parameters[121].

The method employed to characterize a single channel is a so-called EMA. The principle of the EMA is to derive macroscopic approximations from the microscopic layers. In Fig. 8.5 SEM images are presented showing the top side of an IGBT chip and a FIB cut into a single transistor channel.

The FIB cut outlines the geometry of a single transistor channel. By applying energy dispersive X-ray spectroscopy (EDX) as well as knowledge of trench gate IGBTs the varying materials are identified. From the top of Fig. 8.5 a $4\mu m$ Al metallization is observed connecting all the IGBTs placed in parallel. Below the metallization the silicon based emitter

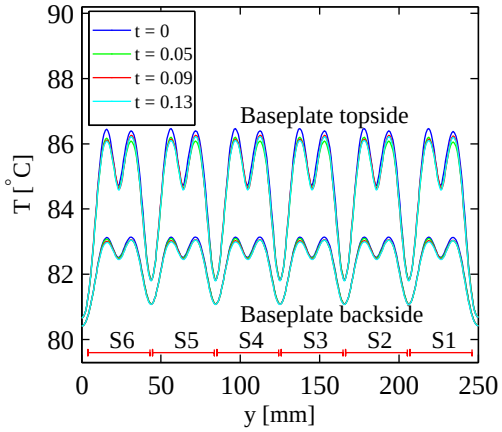


Figure 8.4: Line plot of baseplate topside and backside temperature at module centre at selected times during a power cycle - from paper F.

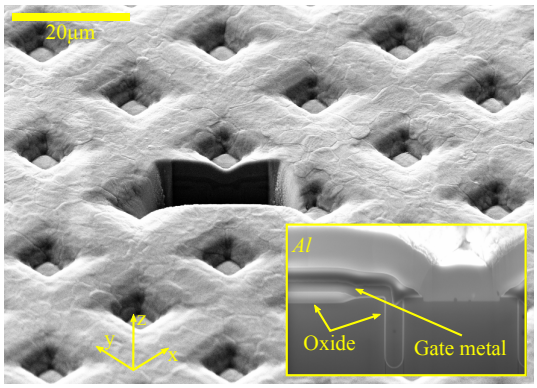


Figure 8.5: SEM images of a FIB cut and a part of the top side of an IGBT chip - from paper F.

channel is situated between the two gates which are separated by an oxide. In Fig. 8.6 a standard trench gate IGBT geometry is depicted. The IGBT depicted may differ from the one shown in Fig. 8.5 but the overall concept should be the same.

In the following the $n+$ layer below the emitter is left out. The remaining is separated

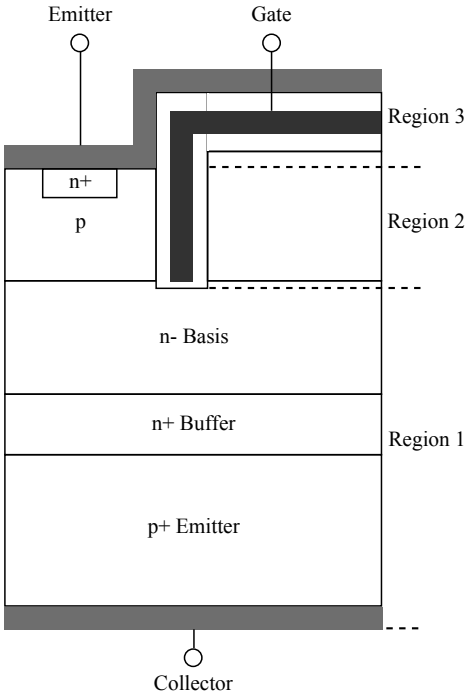
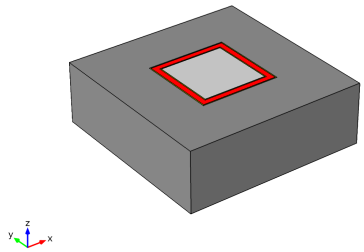


Figure 8.6: Schematic of the layers present in a IGBT. The layout is from [20, p.51].

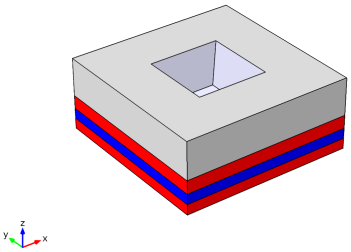
into three regions in a similar way as presented in [121]. Region 2 and 3 are depicted in Figs. 8.7.

1. The first region is handled as one solid doped *Si* crystal. Layers from the collector and until the $n-$ basis layer is included.
2. The second region includes the p layer, the trench gate structure and the vertical oxide.
3. The third region includes the remaining layers, the horizontal gate and oxide as well as the *Al* metallization seen in Fig. 8.5.

The evaluation of the effective physical parameters are carried out through a thermostatic simulation, meaning Eq. (7.22) is solved in the stationary limit. As seen in Fig. fig:regions the regions are in a cubic form which is utilized to solve the thermostatic problem in all



(a) Region 2 - p-doped silicon emitter channel (dark gray) surrounded by oxide (red), trench gate structure (blue) and n- doped basis (dark grey).



(b) Region 3 - aluminum metallization (light grey) on top of oxide layers (red) as well as the horizontal gate structure (blue). The emitter channel from region 2 are still in the middle.

Figure 8.7: CAD illustration of region 2 and 3 for FEM simulation of physical parameters of the transistor.

spatial directions. The spatial directions are isolated from each other so the heat flux from one surface to another may be written from Fourier's law, see Eq. (7.10)

$$q_x = -k_x A \frac{\Delta T}{\Delta x}.$$

So that the average thermal conductivity may be derived as:

$$k_x = -q_x \frac{\Delta x}{A \Delta T}$$

In Fig. 8.8 the problem is sketched.

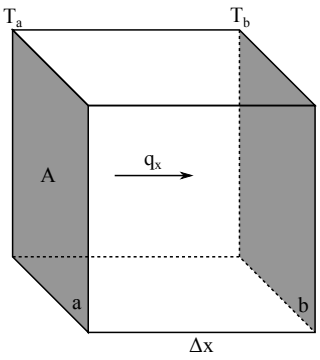
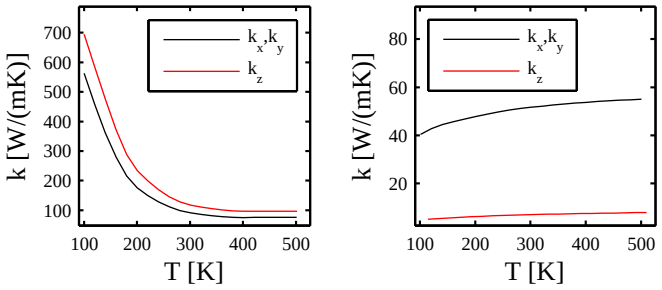


Figure 8.8: Illustration of heat transfer through a rectangular structure of length Δx and cross-sectional area A.

Only one spatial direction is regarded at a time, so the problem is limited to the boundaries a and b. Meaning that the remaining boundaries, which are parallel to the flux direction, are kept strictly adiabatic. By fixing the temperature at b to T_b through a Dirichlet BC, see [91], and applying a given heat flux through a, then k_x as a function of the average temperature may be derived. In Figs. 8.9 the thermal conductivity for the various directions are plotted for region two and three. The parameters in the x and y direction are the same due to symmetry.



(a) Thermal conductivity of region 2, due to symmetry k_x equals k_y.

(b) Thermal conductivity of region 3, the layered structure makes the difference between k_x, k_y and k_z significant.

Figure 8.9: Thermal conductivity of regions 2 and 3 illustrated in figures 8.7(a) and 8.7(b). The orientation of the Cartesian coordinate system is specified in 8.7. From paper F.

In a similar way the specific heat capacity may be derived. Through the specific heat capacity of the individual layers times its mass, a mass-weighted specific heat is obtained:[121]

$$c_{region} = \frac{\sum_i c_i m_i}{\sum_i m_i}$$

So the specific heat capacity of the various layers becomes:

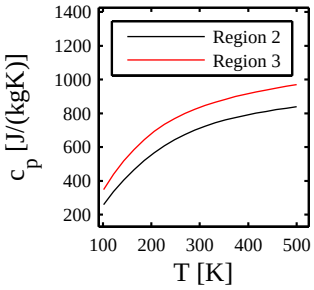
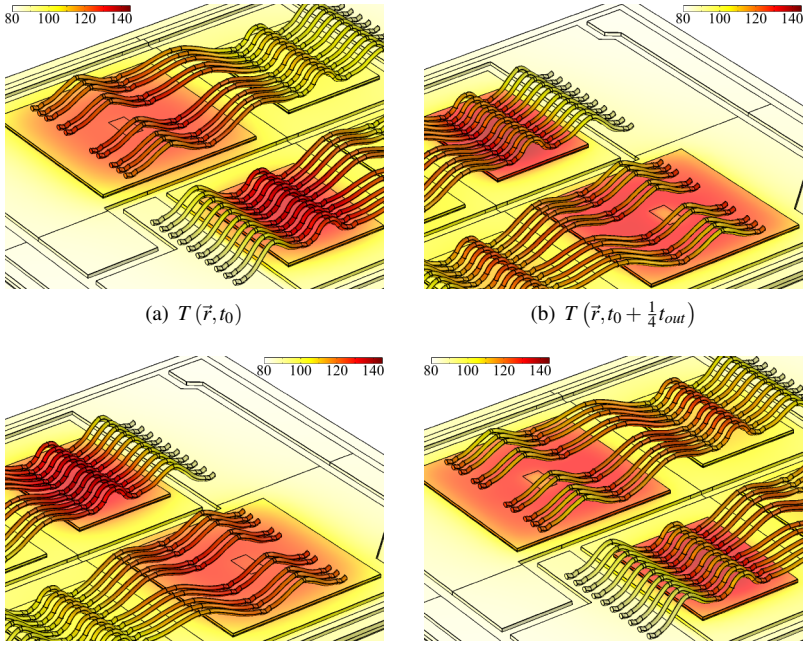


Figure 8.10: Specific heat capacity for region 2 and 3 - from paper F.

8.1.2 Temperature Field

Based on the theory and approximations introduced in previous sections a full time-resolved temperature field may be derived for any type of loading for a full power module. In Figs. 8.11 the temperature field at different time steps under the specification listed in Table 3.1 are presented. The figures are focused on the active regions in the given part of the power cycle.



(a) $T(\vec{r}, t_0)$ (b) $T\left(\vec{r}, t_0 + \frac{1}{4}t_{out}\right)$

(c) $T\left(\vec{r}, t_0 + \frac{2}{4}t_{out}\right)$ (d) $T\left(\vec{r}, t_0 + \frac{3}{4}t_{out}\right)$

Figure 8.11: Temperature fields of power module section at different times during a single power cycle - from paper F.

As expected a clear tendency of an uneven temperature distribution across the chip surface is observed[9, 121]. This is attributed to uneven current distribution, see Fig. 7.3 and higher thermal impedance in specific regions. As will be clear from the thermo-mechanical simulations this creates an increased load on specific wire bonds.

In Fig. 8.12 the mean junction temperature of the four active components are presented, illustrating the increased thermal load on the section diodes.

8.2 Plastic Strain and Material Degradation

By combining the temperature fields presented in Sec. 8.1.2 with the elasto-plastic theory in Sec. 7.3.2 the local strain around any interface of the geometry presented in Fig. 8.2 may be obtained. If additionally, the temperature and strain field are inserted into the material damage model introduced in Sec. 7.4.3 one obtains the degradation parameter around the region of interest.

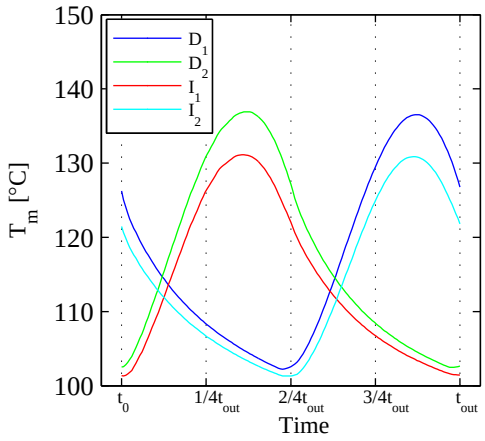


Figure 8.12: Mean junction temperature under sinusoidal loading conditions - from paper F.

8.2.1 Strain and Degradation Field Analysis

In Fig. 8.13 the mean temperature of six wire bond (*wb*) interfaces on top of the LS IGBT is presented. In general, the second bond wb_{i2} (furthest from the diode) has a lower mean temperature indicating a lower peak thermal stress. Additionally, the mean temperature is seen to drop from w_5 and outwards to w_1 as discussed earlier. However, the ΔT is not decreasing in the same way, w_5 is still stressed additionally compared to w_3 and w_1. But the second wire bond is cooling down faster due to further distance from the diode. Exact ΔT values are presented in Figs. 8.15(a)-8.15(f).

In Figs. 8.14 the effective plastic strain increment along a line in parallel to the wire curvature from heel to toe is plotted for one power cycle for wire 1. Even though the mean temperature difference between the two bonds is marginal, see Fig. 8.13, the strain increment is significant. In fact the ΔT is significantly higher in wb_{12}. This is attributed to the contribution from wire flexing of the long wire curve between IGBT and diode.

From the effective plastic strain and the temperature field the differential equation in Eq. (7.49) may be defined and solved for any given boundary. In Figs. 8.15(a)-8.15(f) the degradation function of $wb_{11} - wb_{52}$ whose mean temperature are in Fig. 8.13 are presented. The degradation function is plotted along the same cross-interface line parallel to the wire curvature used in Fig. 8.14.

A similar situation to the difference in plastic strain observed between wb_{11} and wb_{12} in Fig. 8.14 in spite of limited temperature difference, is also seen in the degradation function. Wire 5 experiences the highest mean temperature and temperature variation, of the three, but the degradation function increases more in wb_{31} and the heel of wb_{32}. Again this is accredited to the wire flexing which is supported by the higher damage level in the toe of wb_{52} created by the higher temperature. This illustrate the necessity to include local temperature

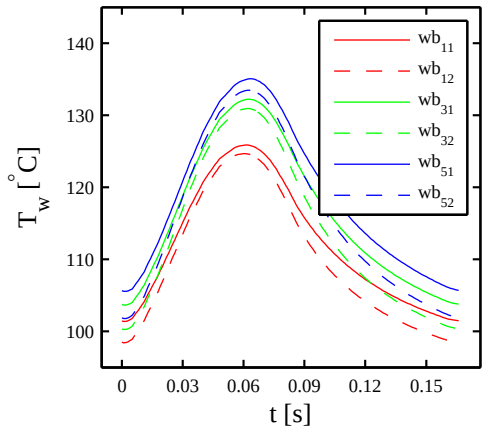
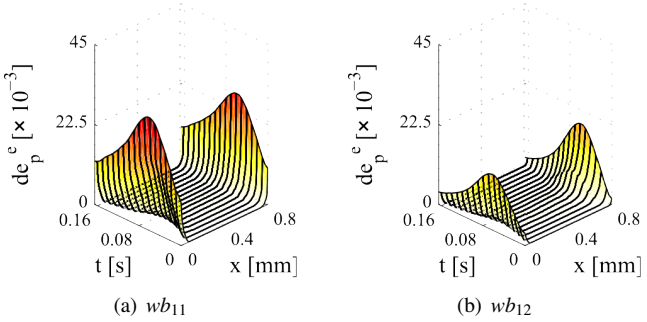
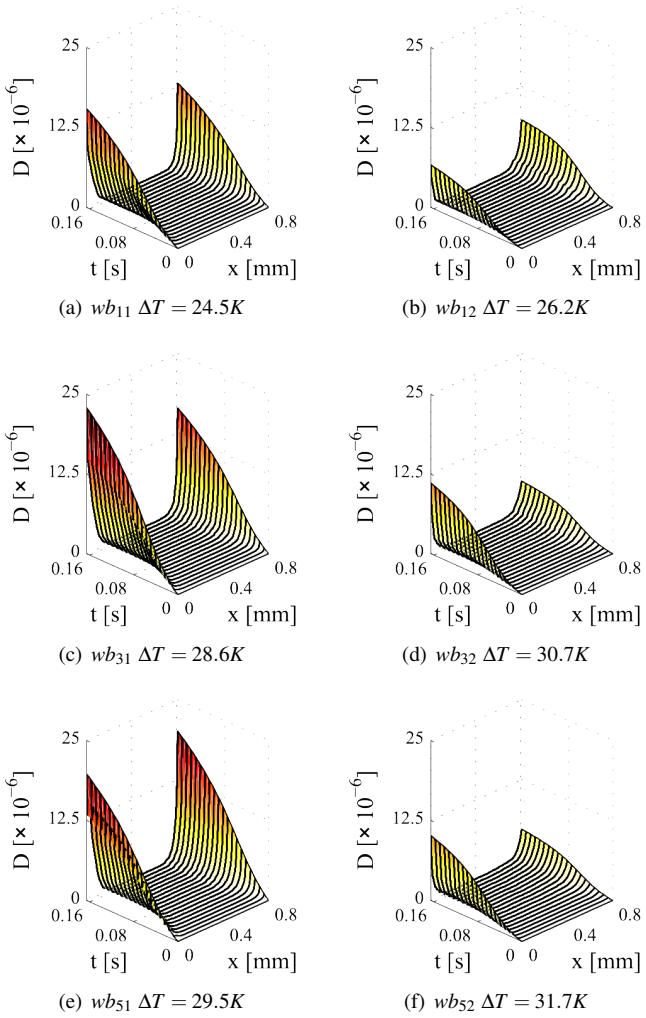


Figure 8.13: Mean temperature of first and second wire bond interface of wires 1,3, and 5 on top of LS IGBT.



(a) wb_{11} (b) wb_{12}

Figure 8.14: Plastic strain increment for both bonds of wire 1 - from paper F.



(a) wb_{11} $\Delta T = 24.5K$ (b) wb_{12} $\Delta T = 26.2K$

(c) wb_{31} $\Delta T = 28.6K$ (d) wb_{32} $\Delta T = 30.7K$

(e) wb_{51} $\Delta T = 29.5K$ (f) wb_{52} $\Delta T = 31.7K$

Figure 8.15: Degradation distribution of IGBT wire bonds of wire 1, 3, and 5 - from paper F.

in the stress/damage analysis instead of only ΔT and mean temperature.

8.2.2 Degradation Model Lifetime Analysis

If one specify a hypothetical wire bond structure (e.g. a typical end bond), and utilize the mean chip junction temperature, depicted in Fig. 8.12, together with the analytical approximations for the plastic strain calculation, presented in Eqs. (7.44) and (7.46), one has a model suited for end of life estimation. This has been carried out for the mean temperature curve presented in Fig. 8.12, with the degradation functions peak value near the heel plotted in Fig. 8.16.

As expected from the load conditions, and shown experimentally in Part II, the diode

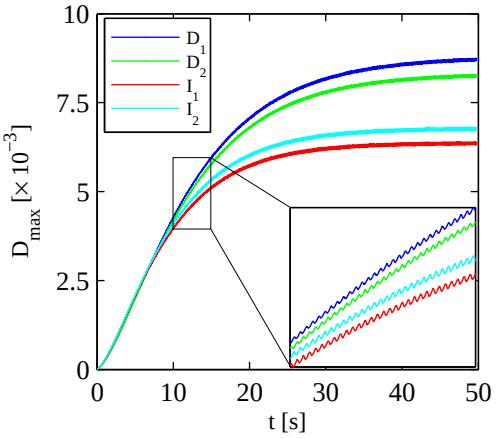


Figure 8.16: Degradation functions peak value near interface heel derived from analytical approximation - from paper F.

wire bonds are degrading at significantly increased speed compared to the IGBT wire bonds. The approach to derive an expected lifetime from the curves in Fig. 8.16 is to specify a crack propagation criteria. So when D reaches a given value a crack is allowed to propagate a given distance. Specification of propagation rate and criteria may be obtained from mechanical tests[17], or if one wants to assess change in physical parameters, by four-point probing as in Fig. 4.8.

Conclusions and Perspectives

As specified in the introduction and thesis summary, the main motivation for the work carried out was to increase the level of understanding of package related failure mechanisms. The reason for this was to enable integration of more physics-of-failure related concepts in design, fabrication, and damage assessment.

In order to accomplish this a number of characterization and testing methods were developed with a focus on combining micro-scale techniques with real life conditions. The scale of required work limited the regarded failure mechanisms to primarily bond wire related and to some degree metallization reconstruction effects. The latter was primarily carried out as a side project in order to investigate its connection with bond wire fatigue. Through the significant amount of investigations concerning wire fatigue issues, a high level of understanding of the micro-scale fracture process as well as macro-scale effects on the module forward voltage has been obtained. This has enabled a formulation of a detailed degradation model able to assess design quality, degradation distribution, and if combined with experimental results - lifetime estimation.

To further improve the results, additional work has to be carried out regarding other package related mechanisms in present designs (solder issues, metallization, ceramic fractures), but also upcoming generations of power modules (sintering, *Cu* wires, integrated systems, etc.). To accomplish this the used characterization techniques needs to be automatized additionally, and theoretical models describing other effects (solder creep, diffusion) must be implemented. Especially concerning metallization reconstruction, test methods without electrical loading must be developed in order to rule out migration effects. This could be accomplished through passive heating from either a heat element or thermal radiation. On top of this non-damaging micro-scale investigations combined with placing devices back into operation would significantly help to understand degradation evolution. Furthermore, it would rule out problems with manufacturing variation from the results. Ways of accomplishing this could be to conduct four-point probing measurements through the power module gel or use non-damaging scanning techniques through material layers.

Additionally, an implementation of physics-of-failure based concepts earlier in the design and fabrication phase would highly increase the component robustness and reliability. This makes it possible to plan and fabricate based on specific load conditions and remove issues like under/over designing. A good example of this is the outcome of paper B, where limited investigation of the *Al* wire bonding process created a good overview of pros and cons in modulation of bonding parameters.

Bibliography

[1] W. Kanert. Active cycling reliability of power devices: Expectations and limitations. *Microelectronics Reliability*, 52:2336–2341, 2012. doi: 10.1016/j.microrel.2012.06.031.

[2] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42: 653–667, 2002. doi: 10.1016/S0026-2714(02)00042-2.

[3] ZVEI Robustness Validation Working Group, editor. *Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications*. ZVEI, 2013. URL `www.zvei.org`.

[4] Hua Lu, Chris Bailey, and Chunyan Yin. Design for reliability of power electronics modules. *Microelectronics Reliability*, 49(9-11):1250 – 1255, 2009. doi: 10.1016/j.microrel.2009.07.055.

[5] J. Lutz, U. Scheuermann, H. Schlangenotto, and R. D. Doncker. *Semiconductor Power Devices - Physcis, Characteristics, Reliability*. Springer-Verlag, 2011. ISBN: 978-3-642-11124-2.

[6] J.M. Guerrero, F. Blaabjerg, T. Zhelev, K. Hemmes, E. Monmasson, S. Jemei, M.P. Comech, R. Granadino, and J.I. Frau. Distributed generation: Toward a new energy paradigm. *Industrial Electronics Magazine, IEEE*, 4(1):52–64, March 2010. doi: 10.1109/MIE.2010.935862.

[7] Rasmus Ørndrup Nielsen, Jens Due, and Stig Munk-Nielsen. Innovative measuring system for wear-out indication of high power IGBT modules. In *IEEE Energy Conversion Congress and Exposition*, pages 1785–1790, 2011. doi: 10.1109/ECCE.2011.6064000.

[8] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H Poech. Fast power cycling test for IGBT modules in traction application. *Power Electronics and Drive Systems*, pages 425–430, 1997. doi: 10.1109/PEDS.1997.618742.

[9] O. Schilling, M. Schfer, K. Mainka, M. Thoben, and F. Sauerland. Power cycling testing and fe modelling focussed on Al wire bond fatigue in high power IGBT modules. *Microelectronics Reliability*, 52:2347–2352, 2012. doi: 10.1016/j.microrel.2012.06.095.

[10] M. Ciappa, P. Malberti, W. Fichtner, P. Cova, L. Cattani, and F. Fantini. Lifetime extrapolation for IGBT modules under realistic operation conditions. *Microelectronics Reliability*, 39:1131–1136, 1999. doi: 10.1016/S0026-2714(99)00160-2.

[11] U.Scheuermann and U.Hecht. Power cycling lifetime of advanced power modules for different temperature swings. *PCIM Nuremberg*, pages 59–64, 2002.

[12] U. Scheuermann and R. Schmidt. Impact of load pulse duration on power cycling lifetime of Al wire bonds. *Microelectronics Reliability*, 53:1687–1691, 2013. doi: 10.1016/j.microrel.2013.06.019.

[13] R. Amro, J. Lutz, and A. Lindemann. Power cycling with high temperature swing of discrete components based on different technologies. In *Power Electronics Specialists Conference*, volume 4, pages 2593–2598, 2004. doi: 10.1109/PESC.2004.1355239.

[14] C. Busca, Remus Teodorescu, Frede Blaabjerg, Stig Munk-Nielsen, L. Helle, T. Abeyasekera, and P. Rodriguez. An overview of the reliability prediction related aspects of high power IGBTs in wind power applications. *Microelectronics Reliability*, 51:1903–1907, 2011. doi: 10.1016/j.microrel.2011.06.053.

[15] I. F. Kovačević, U. Drofenik, and J. W. Kolar. New physical model for lifetime estimation of power modules. In *Proceedings of the International Power Electronics Conference*, pages 2106–2114, 2010.

[16] L. Yang, P. A. Agyakwa, and C. M. Johnson. Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules. *IEEE Transactions on Device and Materials Reliability*, 13: 9–17, 2013. doi: 10.1109/TDMR.2012.2235836.

[17] L. Yang, P. A. Agyakwa, and C. M. Johnson. A time-domain physics-of-failure model for the lifetime prediction of wire bond interconnects. *Microelectronics Reliability*, 51:1882–1886, 2011. doi: 10.1016/j.microrel.2011.07.052.

[18] Arendt Wintrich, Ulrich Nicolai, Werner Tursky, and Tobias Reimann. *Application Manual Power Semiconductors*. SEMIKRON International GmbH, 2011. ISBN: 978-3-938843-66-6.

[19] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani. Ageing and failure modes of igbt modules in high-temperature power cycling. *Industrial Electronics, IEEE Transactions on*, 58(10):4931–4941, Oct 2011. ISSN 0278-0046. doi: 10.1109/TIE.2011.2114313.

[20] A. Volke and M. Hornkamp. *IGBT Modules - Technologies, Driver and Application*. Infineon Technologies, 2011. ISBN: 978-3-00-032076-7.

[21] Y. Nishimura, M. Oonota, and F. Momose. Thermal management technology for IGBT modules. *Fuji Electric Review*, 56(2):79–83, 2010. URL `http://www.fujielectric.com/company/tech/pdf/56-02/FER-56-2-079-2010.pdf`.

[22] V. Smet, F. Forest, J. Huselstein, A. Rashed, and F. Richardeau. Evaluation of vce monitoring as a real-time method to estimate aging of bond wire-igbt modules stressed by power cycling. *Industrial Electronics, IEEE Transactions on*, 60(7):2760–2770, July 2013. ISSN 0278-0046. doi: 10.1109/TIE.2012.2196894.

[23] P.A. Agyakwa, M.R. Corfield, L. Yang, J.F. Li, V.M.F. Marques, and C.M. Johnson. Microstructural evolution of ultrasonically bonded high purity al wire during extended range thermal cycling. *Microelectronics Reliability*, 51(2):406 – 415, 2011. ISSN 0026-2714. doi: 10.1016/j.microrel.2010.08.018.

[24] Ute Geißler, Martin Schneider-Ramelow, Klaus-Dieter Lang, and Herbert Reichl. Investigation of microstructural processes during ultrasonic wedge/wedge bonding of alsi1 wires. *Journal of Electronic Materials*, 35(1):173–180, 2006. doi: 10.1007/s11664-006-0201-2.

[25] S. Ramminger, P. Trkes, and G. Wachutka. Crack mechanism in wire bonding joints. *Microelectronics Reliability*, 38:1301–1305, 1998. doi: 10.1016/S0026-2714(98)00141-3.

[26] P. Dietrich. Trends in automotive power semiconductor packaging. *Microelectronics Reliability*, 53:1681–1686, 2013. doi: 10.1016/j.microrel.2013.07.088.

[27] A. Hamidi, N. Beck, K. Thomas, and E. Herr. Reliability and lifetime evaluation of different wire bonding technologies for high power {IGBT} modules. *Microelectronics Reliability*, 39(6-7):1153 – 1158, 1999. doi: 10.1016/S0026-2714(99)00164-X.

[28] J. E. Krzanowski. A transmission electron microscopy study of ultrasonic wire bonding. *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, 13(1):176–181, March 1990. doi: 10.1109/33.52867.

[29] I. Lum, M. Mayer, and Y. Zhou. Footprint study of ultrasonic wedge-bonding with aluminum wire on copper substrate. *Journal of Electronic Materials*, 35:433–442, 2006. doi: 10.1007/BF02690530.

[30] U. Geißler, M. Schneider-Ramelow, and H. Reichl. Hardening and softening in alsi1 bond contacts during ultrasonic wire bonding. *IEEE Transactions on Components and Packaging Technologies*, 32:794–799, December 2009. doi: 10.1109/TCAPT.2008.2009930.

[31] G. G. Harman and J. Albers. The ultrasonic welding mechanism as applied to aluminium- and gold-wire bonding in microelectronics. *IEEE Transactions on Parts, Hybrids and Packaging*, 13(4):406 – 412, 1977. doi: 10.1109/TPHP.1977.1135225.

[32] B. Langenecker. Effects of ultrasound on deformation characteristics of metals. *IEEE Transactions on Sonics and Ultrasonics*, 13(1):1–8, March 1966. doi: 10.1109/T-SU.1966.29367.

[33] M. A. Occhionero, K. P. Fennessy, R. W. Adams, and G.J Sundberg. AlSiC baseplates for power IGBT modules: design, performance and reliability. 2001. URL `{AlSiC}baseplatesforpower{IGBT}modules:design,performanceandreliability`.

[34] F. P. Incropera, D. P. Dewitt, T. L. Bergman, and A. S. Lavine. *Fundamentals of Heat and Mass Transfer*. John Wiley & Sons, 2007. ISBN: 978-0-471-45728-2.

[35] M. Ciappa and A. Castellazzi. Reliability of high-power igbt modules for traction applications. In *Reliability physics symposium*, pages 480–485, April 2007. doi: 10.1109/RELPHY.2007.369938.

[36] Baozhen Li, Cathryn Christiansen, Dinesh Badami, and Chih-Chao Yang. Electromigration challenges for advanced on-chip cu interconnects. *Microelectronics Reliability*, 54(4):712 – 724, 2014. doi: 10.1016/j.microrel.2014.01.005.

[37] H.R. Zeller. Cosmic ray induced failures in high power semiconductor devices. *Solid-State Electronics*, 38 (12):2041 – 2046, 1995. doi: http://dx.doi.org/10.1016/0038-1101(95)00082-5.

[38] J.W. McPherson. *Reliability Physics and Engineering - Time-To-Failure Modeling*. Springer-Verlag, 2010. doi: 10.1007/978-1-4419-6348-2.

[39] J. Lienig. An introduction to electromigration aware physical design. In *International Symposium on Physical Design (ISPD)*, April 2006.

[40] R. P. Frankenthal and L. F. Garfias-Mesias. *Electronic Materials, Components, and Devices - Uhlig's Corrosion Handbook*. Number 40. Wiley and Sons, third edition, 2011. ISBN: 978-0-470-08032-0.

[41] Wuchen Wu, M. Held, P. Jacob, P. Scacco, and A. Birolini. Investigation on the long term reliability of power igbt modules. In *Power Semiconductor Devices and ICs*, pages 443–448, May 1995. doi: 10.1109/ISPSD.1995.515079.

[42] Y. Celnikier, L. Benabou, L. Dupont, and G. Coquery. Investigation of the heel crack mechanism in al connections for power electronics modules. *Microelectronics Reliability*, 51(5):965 – 974, 2011. doi: 10.1016/j.microrel.2011.01.001.

[43] J. Goehre, M. Schneider-Ramelov, U. Geißler, and K.D. Lang. Interface degradation of Al heavy wire bonds on power semiconductors during active power cycling measured by the shear test. In *Proceedings on Integrated Power Electronics Systems*, number 3.4, pages 1–6, March 2010. ISBN:978-3-8007-3212-8.

[44] Y. Celnikier, L. Dupont, E. Herv, G. Coquery, and L. Benabou. Optimization of wire connections design for power electronics. *Microelectronics Reliability*, 51(9-11):1892 – 1897, 2011. doi: 10.1016/j.microrel.2011.06.058.

[45] B. Czerny, I. Paul, G. Khatibi, and M. Thoben. Experimental and analytical study of geometry effects on the fatigue life of Al bond wire interconnects. *Microelectronics Reliability*, 53(9-11):1558–1562, 2013. doi: 10.1016/j.microrel.2013.07.090.

[46] Eckart Hoene, Andreas Ostmann, Binh The Lai, and Christoph Marczok. Ultra-low-inductance power module for fast switching semiconductors. In *8th International Conference on Integrated Power Electronics Systems*, 2014. ISBN: 978-3-8007-3578-5.

[47] K. Guth, D. Siepe, J. Görlich, H. Torwesten, R. Roth, F. Hille, and F. Umbach. New assembly and interconncects beyond sintering methods. In *PCIM Europe*, pages 232–237, 2010. ISBN: 9781617389672.

[48] Jacek Rudzki, Martin Becker, Ronald Eisele, Max Poech, and Frank Osterwald. Power modules with increased power density and reliability using cu wire bonds on sintered metal buffer layers. In *Integrated Power Systems (CIPS), 2014 8th International Conference on*, pages 1–6, Feb 2014.

[49] S. Pietranico, S. Lefebvre, S. Pommier, M. B. Bouaroudj, and S. Bontemps. A study of the effect of degradation of the aluminium metallization layer in the case of power semiconductor devices. *Microelectronics Reliability*, 51:1824–1829, 2011. doi: 10.1016/j.microrel.2011.06.009.

[50] G. Mitic, R. Beinert, P. Klofac, H.J. Schultz, and G. Lefranc. Reliability of aln substrates and their solder joints in {IGBT} power modules. *Microelectronics Reliability*, 39(6-7):1159 – 1164, 1999. doi: 10.1016/S0026-2714(99)00165-1.

[51] L. Ciampolini, M. Ciappa, P. Malberti, P. Regli, and W. Fichtner. Modelling thermal effects of large contiguous voids in solder joints. *Microelectronics Journal*, 30(11):1115–1123, November 1999. doi: 10.1016/S0026-2692(99)00073-7.

[52] G. Z. Wang, Z. N. Cheng, K. Becker, and J. Wilde. Applying anand model to represent the viscoplastic deformation behavior of solder alloys. *Journal of Electronic Packaging*, 123:247–253, September 2001. doi: 10.1115/1.1371781.

[53] Raed A. Amro. Packaging and interconnection technologies of power devices, challenges and future trends. In *World Academy of Science*, volume 49, pages 691–694, 2009.

[54] P. Cova and F. Fantini. On the effect of power cycling stress on {IGBT} modules. *Microelectronics Reliability*, 38(6-8):1347 – 1352, 1998. doi: 10.1016/S0026-2714(98)00081-X. Reliability of Electron Devices, Failure Physics and Analysis.

[55] S. Schuler and U. Scheuermann. Impact of test control strategy on power cycling lifetime. In *Proceedings of PCIM, Europe*, pages 355–360, 2010.

[56] K.C. Norris and A.H. Landzberg. Reliability of controlled collapse interconnections. *IBM Journal of Research and Development*, 13(3):266–271, May 1969. doi: 10.1147/rd.133.0266.

[57] Kuan-Jung Chung, LiYu Yang, Bing-Yu Wang, and Chia-Che Wu. The investigation of modified norris-landzberg acceleration models for reliability assessment of ball grid array packages. In *Microsystems Packaging Assembly and Circuits Technology Conference*, pages 1–4, Oct 2010. doi: 10.1109/IMPACT.2010.5699640.

[58] Reinhold Bayerer, Tobias Herrmann, Thomas Licht, Josef Lutz, and Marco Feller. Model for power cycling lifetime of igbt modules various factors influencing lifetime. In *Integrated Power Systems (CIPS), 2008 5th International Conference on*, pages 1–6, March 2008. URL `http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5755669`.

[59] U. Scheuermann and R. Schmidt. A new lifetime model for advanced power modules with sintered chips and optimized Al wire bonds. In *Proceedings of PCIM Europe*, pages 810–817, 2013.

[60] C. Hager. *Lifetime Estimation of Aluminum Wire Bonds based on Computational Plasticity*. PhD thesis, Swiss Federal Institute of Technology, 2000.

[61] M.P. Rodriguez, N.Y.A. Shammas, A.T. Plumpton, D. Newcombe, and D.E. Crees. Static and dynamic finite element modelling of thermal fatigue effects in insulated gate bipolar transistor modules. *Microelectronics Reliability*, 40(3):455 – 463, 2000. doi: 10.1016/S0026-2714(99)00250-4.

[62] Hassen Medjahed, Paul-Etienne Vidal, and Bertrand Nogarede. Thermo-mechanical stress of bonded wires used in high power modules with alternating and direct current modes. *Microelectronics Reliability*, 52(6): 1099 – 1104, 2012. doi: 10.1016/j.microrel.2012.01.013.

[63] L. Merkle, M. Sonner, and M. Petzold. Lifetime prediction of thick aluminium wire bonds for mechanical cyclic loads. *Microelectronics Reliability*, 54(2):417 – 424, 2014. doi: 10.1016/j.microrel.2013.10.009.

[64] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, and P.B. Thogersen. A review on real time physical measurement techniques and their attempt to predict wear-out status of igbt. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–10, Sept 2013. doi: 10.1109/EPE.2013.6634419.

[65] Angel Ruiz de Vega, Pramod Ghimire, Kristian Bonderup Pedersen, Ionut Trintis, Szyzmon Beczckowski, Stig Munk-Nielsen, Bjørn Rannestad, and Paul Bach Thøgersen. Test setup for accelerated test of high power IGBT modules with online monitoring of Vce and Vf voltage during converter operation. In *Proceedings of the International Power Electronics Conference*, pages 2547–2553, 2014. doi: 10.1109/IPEC.2014.6869948.

[66] K. Olesen, R. Bredtmann, and R. Eisele. "ShowerPower" new cooling concept for automotive applications. In *Proceedings of the Automotive Power Electronics*, 2006.

[67] D.L. Blackburn. Temperature measurements of semiconductor devices - a review. In *Semiconductor Thermal Measurement and Management Symposium, 2004. Twentieth Annual IEEE*, pages 70–80, Mar 2004. doi: 10.1109/STHERM.2004.1291304.

[68] R. Schmidt and U. Scheuermann. Using the chip as a temperature sensor - the influence of steep lateral temperature gradients on the vce(t)-measurement. In *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, pages 1–9, Sept 2009.

[69] T. Bruckner and S. Bernet. Estimation and measurement of junction temperatures in a three-level voltage source converter. *Power Electronics, IEEE Transactions on*, 22(1):3–12, Jan 2007. doi: 10.1109/TPEL.2006.886651.

[70] Yantao Song and Bingsen Wang. Survey on reliability of power electronic systems. *Power Electronics, IEEE Transactions on*, 28(1):591–604, Jan 2013. doi: 10.1109/TPEL.2012.2192503.

[71] J. Due, S. Munk-Nielsen, and R. Nielsen. Lifetime investigation of high power igbt modules. In *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pages 1–8, Aug 2011. URL `http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6020272`.

[72] L.B. Valdes. Resistivity measurements on germanium for transistors. *Proceedings of the IRE*, 42(2):420–427, Feb 1954. ISSN 0096-8390. doi: 10.1109/JRPROC.1954.274680.

[73] F.M. Smits. Measurement of sheet resistivities with the four-point probe. *Bell System Technical Journal*, 34: 711–718, May 1958.

[74] G. F. Vander Voort. *ASM Handbook: Volume 9: Metallography And Microstructures*. ASM International, 2004.

[75] E. Cerri and E. Evangelista. Metallography of aluminium alloys. Technical report, Department of Mechanics, University of Ancona, 1999. EAA - European Aluminium Association.

[76] Elisabeth Weidmann and Anne Guesnier. Application notes - metallographic preparation of aluminium and aluminium alloys. Technical report, Struers A/S, 2008.

[77] M. Mohmmadtaheri. A new metallographic technique for revealing grain boundaries in aluminum alloys. *Metallography, Microstructure, and Analysis*, 2012. doi: 10.1007/s13632-012-0033-9.

[78] E. C. W. Perryman and J. M. Lack. Examination of metals by polarized light. *Nature*, 167:479, 1951.

[79] N. Hansen. Hall-petch relation and boundary strengthening. *Scripta Materialia*, 51(8):801–806, 2004. doi: 10.1016/j.scriptamat.2004.06.002.

[80] B. Czerny, M. Lederer, B. Nagl, A. Trnka, G. Khatibi, and M. Thoben. Thermo-mechanical analysis of bonding wires in IGBT modules under operating conditions. *Microelectronics Reliability*, 52:2353–2357, 2012. doi: 10.1016/j.microrel.2012.06.081.

[81] Kristian Bonderup Pedersen, Peter Kjær Kristensen, Vladimir Popok, and Kjeld Pedersen. Interface structure and strength of ultrasonically wedge bonded heavy aluminium wires in Si-based power modules. *Journal of Materials Science: Materials in Electronics*, 25(7):2863–2871, July 2014. doi: 10.1007/s10854-014-1953-8.

[82] M. H. Bierhoff and F. W. Fuchs. Semiconductor losses in voltage source and current source IGBT converters based on analytical deriviation. In *35th Annual Power Electronics Specialties Conference*, pages 2836–2842, 2004.

[83] D. Graovac and Marco Prschel. IGBT power losses calculation using the data-sheet parameters. Technical report, Infinion Automotive Power, January 2009.

[84] A. D. Rajapakse, A. M. Gole, and P. L. Wilson. Approximate loss formulae for estimation of IGBT switching losses through emtp-type simulations. IEEE, 2005.

[85] A.D. Rajapakse, A.M. Gole, and P.L. Wilson. Electromagnetic transients simulation models for accurate representation of switching losses and thermal performance in power electronic systems. *Power Delivery, IEEE Transactions on*, 20(1):319–327, Jan 2005. doi: 10.1109/TPWRD.2004.839726(410) 2.

[86] S.A. Kharitonov, M.A. Petrov, D.V. Korobkov, M.A. Maslov, and T.Y. Zhoraev. A principle of calculation dynamic and static power losses with hard-switching igbt. In *Electron Devices and Materials*, pages 147–149, July 2005. doi: 10.1109/SIBEDM.2005.195608.

[87] M. Rodriguez, A. Rodriguez, P.F. Miaja, D.G. Lamar, and J.S. Zuniga. An insight into the switching process of power mosfets: An improved analytical losses model. *Power Electronics, IEEE Transactions on*, 25(6): 1626–1640, June 2010. doi: 10.1109/TPEL.2010.2040852.

[88] Yali Xiong, Shan Sun, Hongwei Jia, P. Shea, and Z.J. Shen. New physical insights on power mosfet switching losses. *Power Electronics, IEEE Transactions on*, 24(2):525–531, Feb 2009. doi: 10.1109/TPEL.2008.2006567.

[89] C. Martin, J.-L. Schanen, J.-M. Guichon, and R. Pasterczyk. Analysis of electromagnetic coupling and current distribution inside a power module. *Industry Applications, IEEE Transactions on*, 43(4):893–901, July 2007. doi: 10.1109/TIA.2007.900453.

[90] A. D. Kraus. *Basic Concepts - Heat Transfer Handbook*. Wiley and Sons, 2003.

[91] A. Aziz. *Conduction of Heat Transfer - Heat Transfer Handbook*. Wiley and Sons, 2003.

[92] R. Codina. Comparison of some finite element methods for solving the diffusion-convection-reaction equation. *Computer Methods in Applied Mechanics and Engineering*, 156(1-4):185–210, April 1998. doi: 10.1016/S0045-7825(97)00206-5.

[93] Y. Joshi and W. Nakayama. *Forced Convection: External Flows - Heat Transfer Handbook*. Wiley and Sons, 2003.

[94] Y. Jaluria. *Natural Convection - Heat Transfer Handbook*. Wiley and Sons, 2003.

[95] M. M. Yovanovich. Micro and macro hardness measurements, correlations, and contact models. 44th AIAA Aerospace Sciences Meeting and Exhibit, 2006. URL `http://www.mhtl.uwaterloo.ca/pdf_papers/mhtl06-2.pdf`.

[96] W.T. Becker and S. Lampman. Fracture appearance and mechanisms of deformation and fracture. *ASM Handbook Volume 11, Failure Analysis and Prevention (ASM International)*, 2002.

[97] H. J. Frost and M. F. Ashby. *Deformation-Mechanism Maps*. Pergamon Press, 1982.

[98] Dominique Francois, Andre Pineau, and Andre Zaoui. *Mechanical Behaviourof Materials - Volume 1: Micro- and Macroscopic Constitutive Behaviour*. Springer-Verlag, 2012. doi: 10.1007/978-94-007-2546-1.

[99] D. Linkens. *Selected Benchmarks for Material Non-Linearity*. NAFEMS, 1993.

[100] T. R. Hsu. *The Finite Element Method in Thermomechanics*. Allen & Unwin Inc., 1986. ISBN: 0-04-620013-4.

[101] Y.K. Lee. A unified framework for compressible plasticity. *International Journal of Plasticity*, 10(6):695 – 717, 1994. doi: 10.1016/0749-6419(94)90029-9.

[102] R. Darveaux. Effect of simulation methodology on solder joint crack growth correlation. In *Electronic Components; Technology Conference Proceedings. 50th*, pages 1048–1058, 2000. doi: 10.1109/ECTC.2000.853299.

[103] W. Bolton. *Mechanical Science*. Blackwell Publishing, 2006. ISBN: 1-4051-3794-0.

[104] M. A. Bhatti. *Fundamental Finite Element Analysis and Applications*. John Wiley & Sons, 2005. ISBN: 0-471-64808-6.

[105] David W . Nicholson. *Finite Element Analysis - Thermomechanics of Solids*. CRC Press, 2008. doi: 10.1201/9781420050974.ch17.

[106] R. M. Richard and J. R. Blacklock. Finite element analysis of inelastic structures. *AIAA Journal*, 7(3): 432–438, 1969. doi: 10.2514/3.5125.

[107] C. Hager, Y. Tronel, and W. Fichtner. Electro-thermo-mechanical simulations of aluminum bond wires in IGBT-packages. *Technical Proceedings of the 1998 International Conference on Modelling and Simulation of Microsystems*, pages 163–167, 1998.

[108] N. Hansen and X. Huang. Microstrucure and flow stress of polycrystals and single crystals. *Acta materials*, 46:1827–1836, 1998.

[109] Y. Verreman and G. Espinosa. Mechanically short crack growth from notches in a mild steel. *Fatigue & Fracture of Engineering Materials & Structures*, 20(2):129–142, 1997. doi: 10.1111/j.1460-2695.1997.tb00273.x.

[110] Dominique Francois, Andre Pineau, and Andre Zaoui. *Mechanical Behaviourof Materials - Volume 2: Fracture Mechanics and Damage*. Springer-Verlag, 2013. doi: 10.1007/978-94-007-4930-6.

[111] D. Sornette, T. Magnin, and Y. Brechet. The physical origin of the coffin-manson law in low-cycle fatique. *Europhysics Letters*, 20(5):433–438, 1992. doi: 10.1209/0295-5075/20/5/009.

[112] R. T. Jacobsen, E. W. Lemmon, S. G. Penoncello, Z. Shan, and N. T. Wright. *Thermophysical Properties of Fluids and Materials - Heat Transfer Handbook*. Wiley and Sons, 2003.

[113] R. Winston Revie, editor. *Uhlig's Corrosion Handbook*. Wiley and Sons, third edition, 2011. ISBN: 978-0-470-08032-0.

[114] James F . Shackelford and William Alexander, editors. *CRC Materials Science and Engineering Handbook*. CRC Press, third edition, 2000. ISBN: 978-0-8493-2696-7.

[115] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson. Thermal conduction in doped single-crystal silicon films. *Journal of Applied Physics*, 91(8):5079–5088, 2002. doi: 10.1063/1.1458057.

[116] G. Slack. The intrinsic thermal conductivity of AIN. *Journal of Physics and Chemistry of Solids*, 48: 641–647, 1987. doi: 10.1016/0022-3697(87)90153-3.

[117] V. L. Koshchenko, Y. K. Grinberg, and A. F Demidenko. *Inora. Mater.*, 20(11):1550–1553, 1984.

[118] Thomas Siewert, Stephen Liu, David R. Smith, and Juan Carlos Madeni. Database for solder properties with emphasis on new lead-free solders. Technical report, National Institute of Standards and Technology, 2002. URL `http://www.msed.nist.gov/solder/NIST_LeadfreeSolder_v4.pdf`.

[119] MatWeb. URL `http://matweb.com/`.

[120] J. Wilde, W. Staiger, and M. Thoben. An integrated design approach for the hardware optimization of electrical power modules for automotive electrotraction. In *Vehicle Electronics Conference, 1999. (IVEC '99) Proceedings of the IEEE International*, pages 170–178 vol.1, 1999. doi: 10.1109/IVEC.1999.830655.

[121] S. Filippis, H. Köck, M. Nelhiebel, V. Kosel, S. Decker, M. Glavanovics, and A. Irace. Modelling of highly anisotropic microstructures for electro-thermal simulations of power semiconductor devices. *Microelectronics Reliability*, 52:2374–2379, 2012. doi: 10.1016/j.microrel.2012.06.103.